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(54) Manufacturing process of a germanium implanted HBT bipolar transistor

(57) A process for fabricating a vertical structure high carrier mobility transistor on a substrate (1) of crystalline silicon doped with impurities of the N type, having a collector region (2) located at a lower portion of the substrate, the process comprising the steps of:

defining a window (10) in the semiconductor substrate (1);

providing a first implantation of germanium (Ge) atoms through said window (10);

providing a second implantation of acceptor dopants through said window (10) to define a base region;

applying an RTA treatment, or treatment in an oven, to reconstruct the crystal lattice within the semiconductor substrate comprising a silicon/germanium alloy ($Si_{1-x}Ge_x$);

forming a first thin dielectric layer (12) of silicon dioxide (SiO_2) by chemical vapor deposition; depositing a second dielectric layer (14) onto said first dielectric layer (12);

depositing a polysilicon layer (15) onto said second dielectric layer (14);

etching away, within the window region (10), said first (12) and second (14) dielectric layers, and the polysilicon layer (15), to expose the base region (3) and form isolation spacers (50) at the window edges;

forming an N-doped emitter (4) in the base (3) and window regions.

This fabrication process is specially attentive to the formation of the silicon dioxide SiO_2/Ge_xSi_{1-x} interface present in vertical structure HBT transistors, if isolation spacers are to be formed.

The fabrication process of this invention allows the frequency field of application of HBT transistors to be further extended, while eliminating deviations of the base currents from the ideal.

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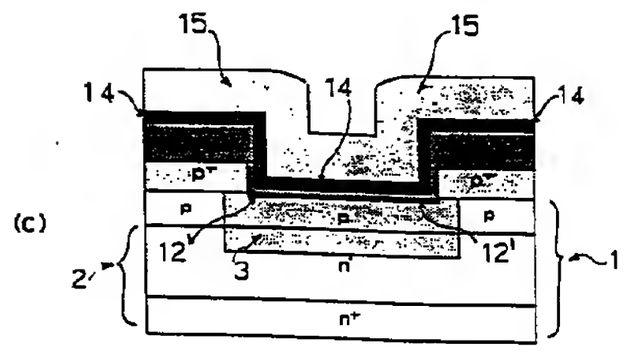
INVENTION



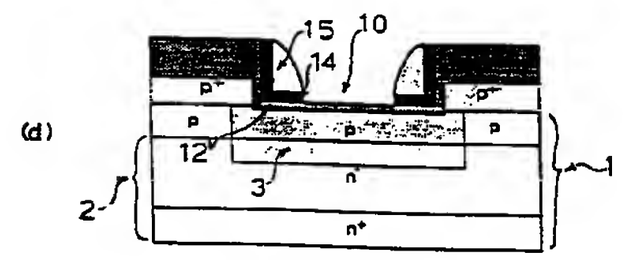
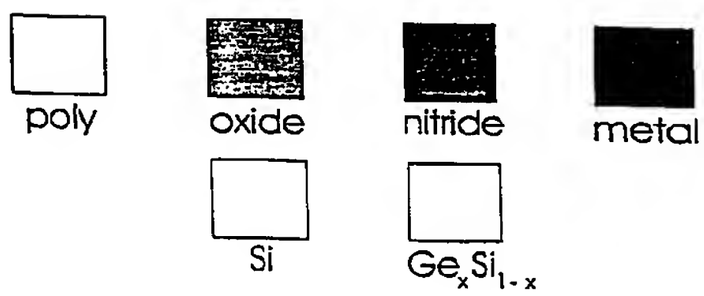


FIGURE 9



Description

Field of the Invention

This invention relates to a process for fabricating a vertical structure high carrier mobility transistor on a crystalline silicon substrate, having a collector region located at a lower portion of the substrate, the process comprising the steps of:

- defining a window in the semiconductor substrate;
- providing a first implantation of germanium (Ge) atoms through said window;
- providing a second implantation of acceptor dopants through said window to define a base region;
- applying an RTA (Rapid Thermal Annealing) treatment to re-construct the crystal lattice within the semiconductor substrate comprising a silicon/germanium alloy ($Si_{1-x}Ge_x$).

The invention relates, particularly but not exclusively, to a process for fabricating a HBT bipolar transistor for very high frequency applications, and the description to follow is given with reference to this applicational field for convenience of illustration.

Background Art

As skilled persons in the art know well, the application of heterostructures to solid state electronic devices has prompted a vast increase of their working range at very high frequencies.

In particular, this technology has been applied to bipolar transistor devices, to thereby improve both the injection efficiency of the charge carriers and the passage frequency (f_t) value, the latter being closely related to the cut-off frequency (f_T) of the device.

Heterostructures can be prepared by different methods, of which the MBE (Molecular Beam Epitaxy) method is the best known and provides a structure free of lattice imperfections; other, more expensive methods are sophisticated versions of CVD which, however, have a disadvantage in that their throughput adds to the cost of the silicon die.

Yet this method has only sparsely been applied to large volume industrial processes, on account of it involving lengthy processing steps that command strict control of their physical parameters.

Thus, it has often been more convenient to adopt other methods, such as ion implantation, which could yield similar heterostructures of a fair quality within acceptable times for large volume production lines.

A bipolar transistor implemented by a vertical structure including a Ge_xSi_{1-x} heterostructure between the base and collector regions will now be described in relation to such a field of application.

The HBT bipolar transistor under consideration is illustrated schematically by the enlarged cross-sectional view of Figure 1.

This HBT transistor has a vertical structure of the NPN type and is formed on a crystalline semiconductor substrate 1 wherein, by successive implantations, a collector region 2 of the N type, base region 3 of the P type, and emitter region 4 of the N type have been defined, from the substrate bottom up.

Specifically, it can be seen that the collector region 2 includes a heavily N-doped layer 5 effective to provide a good Ohmic contact with a collector metal (not shown because conventional) provided in a lower portion of the substrate 1.

An added feature of the HBT transistor shown in Figure 1 is an opening provided above the substrate 1 to isolate the base region 3 and later allow formation of a contact region 9 above the emitter region 4.

This contact region 9 comprises a heavily N-doped layer 7 overlaid by a metal layer 8.

Having briefly described the HBT transistor, the Ge_xSi_{1-x} heterostructure formed within the crystalline silicon substrate 1 will now be examined to see what changes are introduced in the energy band curve of the HBT transistor.

This Ge_xSi_{1-x} heterostructure is characterized by the x and 1-x concentrations, respectively associated with the silicon and germanium atoms, varying with the spatial implant depth in the substrate 1.

In Figure 2, the energy band curve of the bipolar transistor HBT is plotted as a full line for comparison with the band curve of a standard bipolar transistor (BJT), plotted as a broken line.

A comparison of the two band curves of the transistors HBT and BJT shows that the bipolar transistor HBT has an energy level in the conduction band which is always below that of the standard transistor BJT, through the base region to the interface with the collector region.

In particular, it can be seen that for the transistor HBT, when moving from its base region toward its collector region, there occurs a gradual slow decrease of its energy gap (E_g) which can be regarded as an effect of spatial modulation of the energy gap. This modulation is obtained by suitable implantation profiles of the germanium (Ge) atomic species whose concentration is maximal at the collector-base interface and minimal or almost nil at the emitter-base interface.

The active zone bias of the bipolar transistor HBT conforming with the above band curve allows of faster injection of the carriers from the emitter region, thereby greatly reducing their passage time.

The net result is a markedly increased cut-off frequency (f_T) of the HBT transistor and a decreased proportion of carriers trapped within the base.

Thus, for HBT transistors biased with collector cur-

rents in the milliAmpere range, cut-off frequency values can be obtained which would not be achievable by conventional bipolar technology.

The Ge_xSi_{1-x} heterostructure provided between the base and collector regions enables the P-doping of the base region to be increased, thereby lowering the value of the intrinsic resistance R_{bb} in the base region that restricts the applications of bipolar transistors at high frequencies.

A previously mentioned method of conventionally forming the HBT transistor with a Ge_xSi_{1-x} heterostructure will now be described with reference, in particular, to Figures 3a-3f. The same reference numerals used for similar elements in Figure 1 have been retained for convenience.

Figure 3a shows a crystalline silicon substrate 1 which has been doped with impurities of the N type and formed with a window 10 by selective deposition of a protective material 11. This protective material comprises a material layer, including impurities of the P type, which is deposited over the substrate and insulated by a dielectric capping.

A first implantation of germanium (Ge) is carried out through this opening 10, and is followed by a second implantation of acceptor impurities, such as boron (B) atoms or BF_2^+ ions.

Thereafter, a step of re-construction of the crystal lattice of the substrate 1 is carried out by an RTA (Rapid Thermal Annealing) process, or a conventional thermal process in an oven, which is also applied to aid in driving the implanted ions into sites freed in the crystal lattice.

The outcome of this reconstruction step is shown in Figure 3b, where a planar base region 3, extending at the window 10 to a sufficient depth to allow of the subsequent creation of an emitter region, is highlighted for the first time.

Simultaneously with the formation of the base region 3 in the substrate 1, a collector region 2 is defined which is incorporated to the remaining portion, not implanted with P-type impurities, of the substrate 1.

The base region, extending as far as the interface to the collector region 2, will presently feature a Ge_xSi_{1-x} heterostructure formed during the first implanting step and characterized by an energy band curve of the kind shown in Figure 2.

From now on, as shown in Figure 3c, the processing over the substrate 1, at the location of the window 10 and the protective material 11, will see the following successive operations:

- thermal growth of a first thin dielectric layer 12 of silicon dioxide (SiO_2);

- deposition of a second dielectric layer 14, typically of silicon nitride (Si_3N_4), onto the first thin dielectric layer 12;

- deposition of a polysilicon layer 15.

To provide an emitter region at the location of the window 10 in the substrate 1, the process for fabricating the HBT transistor comprises a first chemio-physical etching (RIE) step and a second etching step, respectively of the polysilicon layer 15 and the second dielectric layer 14, to partially form isolation spacers at the edges of the window 10, as shown in Figure 3d.

A third wet etching step of the remaining portions of the polysilicon layer 15, and a fourth etching step of the first thin dielectric layer 12 only, bring to completion the formation of the spacers 50, thereby exposing the base region 3 again, as shown in Figure 3e.

The HBT transistor with Ge_xSi_{1-x} heterostructure can now be completed by conventional processes for the formation of an emitter region 4 accommodated within the base region 3 and overlaid by a corresponding emitter contact 9.

Figure 3f is a general view of the HBT transistor with Ge_xSi_{1-x} heterostructure being provided with an emitter contact 9 which comprises a first polysilicon layer 7 heavily doped with impurities of the N type and metallized on top by a layer 8.

The HBT transistors with Ge_xSi_{1-x} heterojunction fabricated with the above process have revealed upon testing a behavior of the base current which is less than ideal.

This deviation from the ideal is brought out by the graph of Figure 4, where the collector and base currents are plotted versus the voltage V_{be} between the base and the emitter, for two different HBT transistors formed on a common substrate.

The HBT transistors (T1,T2) in question have values (At1,At2) of their emitter surface areas of 2x7.4 μm^2 and 0.4x7.4 μm^2, respectively, resulting in a ratio (At1/At2) of five between their emitter areas and a ratio (pt1/pt2) of 1.2 between the outer perimeters of their emitter regions.

On the graph, the curves relating to the transistor T1 are full lines, and those relating to the transistor T2 are broken lines.

It can be seen from the graph that the base currents (those having flatter curves) of T1 and T2 differ little from each other, although the ratio (At1/At2) of their emitter areas is of five.

This brings out the existence of a non-ideal component for the base current which is unaffected by changes in the emitter surface area. This deviation from the ideal, well recognized in the art, has been attributed heretofore to attempts of the Ge_xSi_{1-x} heterostructure, regarded as being responsible for re-combination phenomena within the semiconductor substrate, to relax.

The technical problem underlying this invention is to provide a process for fabricating a transistor with Ge_xSi_{1-x} heterostructure, which can overcome the limitation described hereinabove so as to further improve its frequency performance.

Summary of the Invention

The solution idea on which this invention stands is to spot the cause for HBT transistors deviating from the ideal among surface re-combination phenomena, rather than recombination phenomena reputedly occurring within the Ge_xSi_{1-x} heterostructure.

Such surface re-combination phenomena have been found to occur in the neighborhood of the interface between the crystalline semiconductor substrate, incorporating a HBT transistor, and a thin layer of silicon dioxide (SiO_2) grown to aid in the formation of the spacers near an emitter region.

Based on this solution idea, the technical problem is solved by a process as previously indicated and defined in the characterizing parte of Claim 1.

The features and advantages of the process according to the invention will be apparent from the following description of an embodiment thereof, given by way of non-limitative example with reference to the accompanying drawings.

Brief Description of the Drawings

In the drawings:

Figure 1 is an enlarged cross-sectional view of a semiconductor substrate which integrates a high-mobility NPN transistor with a vertical structure including a Ge_xSi_{1-x} heterostructure, according to the prior art;

Figure 2 is an energy band plot typical of a high-mobility NPN transistor;

Figures 3a-3f illustrate conventional process steps yielding the high-mobility NPN transistor shown schematically in Figure 1;

Figure 4 is a voltage vs. current plot illustrating the behavior of the base and collector currents for two high-mobility NPN transistors T1 and T2 with a Ge_xSi_{1-x} heterostructure having a ratio At1/At2 of 5 of their respective emitter areas;

Figure 5 is an enlarged cross-sectional view of a semiconductor body of crystalline silicon as implanted to provide a Ge_xSi_{1-x} heterostructure, which has been subjected to an oxidation step for growing a silicon dioxide layer thereon;

Figure 6 is a photograph taken by Atomic Force Microscopy (AFM), which shows an SiO_2/Ge_xSi_{1-x} interface of a conventionally made transistor;

Figure 7 is a plot illustrating the dependence of surface roughness at an SiO2/GexSi1-x interface on the amount of germanium segregated in the interface itself;

Figure 8 illustrates a similar situation to that of Figure 7, but relating to a practical instance of a high carrier mobility transistor also having an SiO2/GexSi1-x interface;

Figures 9a-9f illustrate the process steps according to this invention that yield a high-mobility NPN transistor similar to that shown schematically in Figure 1;
two different types of HBT transistors;

Figure 12 is a plot of the collector current versus the collector-emitter bias voltage, for two different types of HBT transistors;

Figure 13 is a plot of the concentration Figure 10 is a photograph taken by Atomic Force Microscopy (AFM), which shows an SiO2/GexSi1-x interface obtained with the fabrication process of this invention;

Figure 11 is a plot showing the behavior of the collector and base currents versus the base-emitter bias voltage, for profiles of acceptor impurities in substrates integrating two different types of HBT transistors;

Figure 14 is a plot of the cut-off frequency versus the collector bias current for two different types of HBT transistors.

Detailed Description

To overcome the technical problem previously discussed under the Background Art heading, the present invention has spotted the main cause of deviations from the ideal which limit, for example, the performance of a high-mobility HBT transistor, in the surface re-combination phenomena that appear at the silicon dioxide-to-germanium/silicon heterostructure, SiO2/GexSi1-x.

In order to provide experimental evidence of the above, the Applicant has conducted a series of atomic force microscopy (AFM) analyses to photograph the situation at the SiO2/GexSi1-x interface and gather useful elements for evaluation.

These analyses have shown a situation of the kind schematically illustrated in Figure 5, wherein, on a body 30 of crystalline silicon implanted to produce a GexSi1-x heterostructure, a layer 33 of pure germanium develops subsequently to a step of growing a layer 32 of silicon dioxide on the crystalline body 30.

This layer 33 is trapped from beneath by the Ge_xSi_{1-x} heterostructure, and from above, by the silicon dioxide layer 32. This can be explained in theory by that the step of growing the silicon dioxide (SiO_2) thermally, as carried out in direct contact with the GexSi1-x heter-

ostructure, causes the silicon (Si) atoms present at its top surface to be depleted, thereby promoting the formation of the layer 33 of pure germanium.

In so doing, the silicon dioxide layer 32 develops a surface roughness, due to the underlying germanium layer 33, which is responsible for the surface re-combination phenomena occurring at the SiO_2/Ge_xSi_{1-x} interface.

This surface roughness is brought out by the atomic force microphotograph of Figure 6, showing the surface of the silicon dioxide layer 32 after the thermal growth process.

Figure 7 is a plot showing the linearly increasing dependence of the amount of segregated germanium in the layer 33 on the surface roughness (Rms) of the layer 32.

A similar situation to the above, for an SiO2/GexSi1-x interface, is encountered where a high carrier mobility bipolar transistor (HBT) having a vertical structure with a $_{Gex}Si_{1-x}$ heterostructure is fabricated by the process steps described under the Background Art heading.

Figure 8 is a cross-section through the high-mobility transistor of Figure 1, with enlarged detail views of the emitter 4 and base 3 regions.

This figure highlights that the base and emitter regions are in direct contact with the isolation spacers 50 comprised of a first thin dielectric layer 12 of silicon dioxide and a second dielectric layer 14.

It is to be emphasized, therefore, that a Ge_xSi_{1-x} heterostructure is present within the base region 3 whereover the first thin dielectric layer 12 of silicon dioxide comprising both isolation spacers 50 has been grown.

Accordingly, a narrow region of the SiO_2/Ge_xSi_{1-x} interface has been marked with a heavy circle where the presence is displayed of a layer 90 of segregated germanium resulting from the thermal oxidation process employed for growing the first thin dielectric layer 12.

To overcome the drawbacks connected with the SiO2/GexSi1-x interface which limit the performance of conventional high-mobility transistors (HBT), a process for fabricating the transistor of this invention will be proposed herein below with reference to Figures 9a-9f.

For convenient comparison of the inventive process with the process described under the Background Art heading, the same reference numerals have been used to denote identical items with those shown in Figures 1 and 3a-3f.

Figure 9a shows a substrate 1 of crystalline silicon (Si), lightly doped with impurities of the N type and having a bottom region 5 which is heavily doped with impurities of the N type. This region 5 corresponds to the Ohmic region of the collector contact (not shown here).

A window 10 is formed above the substrate 1 by selective deposition of a protective material 11 over the substrate 1. This protective material comprises a first layer in direct contact with the substrate 1 wherein acceptor impurities are embedded and which is capped by a dielectric material.

A first step of implanting germanium (Ge) is carried out through this opening 10, followed by a second step of implanting acceptor impurities, such as boron (B) atoms or BF2+ ions.

Thereafter, the crystal lattice of the substrate 1 is reconstructed by an RTA (Rapid Thermal Annealing) process or a conventional treatment in the oven, also intended to aid in the insertion of the implanted atoms into the sites left free in the crystal lattice.

The outcome of the last-mentioned step is shown in Figure 9b, where a planar base region 3, extending at the window 10 to a sufficient depth in the substrate 1 to allow of the subsequent creation of an emitter region, is highlighted for the first time.

Simultaneously with the definition of the base region 3 in the substrate 1, a collector region 2 is defined which is included in the remaining portion, not implanted with acceptor impurities, of the substrate 1 and, accordingly, also contains the collector Ohmic contact region 5.

The base region, extending as far as the interface to the collector region 2, will presently exhibit an energy band curve of the kind shown in Figure 2 as a result of a Ge_xSi_{1-x} heterostructure having been formed during the first implanting step.

At this stage, as shown in Figure 9c, at the location of the window 10 and the protective material 11, a first thin dielectric layer 12' of silicon dioxide (SiO_2) will be formed over the substrate 1 by chemical vapor deposition (CVD). Other techniques, such as PECVD, APCVD, LPCVD, UV-assisted CVD, could be used.

Unlike the prior art, this thin dielectric layer 12' of silicon dioxide is formed by a CVD process, not by thermal growth.

This provides an improved SiO_2/Ge_xSi_{1-x} interface, as can be seen in Figure 10 which shows an atomic force microphotograph of the $SiO2/Ge_xSi_{1-x}$ interface thus obtained.

It can be seen that the roughness of the $SiO2/Ge_xSi_{1-x}$ interface is significantly less than in Figure 6 where the silicon dioxide was grown by thermal oxidation.

Excellent results, as regards the formation of the $SiO2/Ge_xSi_{1-x}$ interface, were obtained by depositing the first thin dielectric layer 12' of silicon dioxide by an atmospheric pressure chemical vapor deposition (APCVD) process.

To further enhance the quality of the interface, and thus reduce the faults originating local surface re-combination phenomena. it is contemplated that a thermal process should follow the deposition of the first thin dielectric layer 12'.

The process for fabricating a HBT transistor according to the invention is carried on through conventional steps including the deposition of a second dielectric layer 14 on top of said first thin dielectric layer 12', fol-

lowed by the deposition of a polysilicon layer 15.

In an alternative embodiment, the second dielectric layer comprises silicon nitride ($_{Si3}N_4$) to ensure proper adhesion on the underlying layer 12'.

Finally, to form an emitter region in the substrate 1, at the location of the window 10, a first chemio-physical etching (RIE) step will be carried out on the polysilicon layer 15, and a second etching step on the second dielectric layer 14, to obtain the partial formation of isolation spacers at the edges of the window 10, as shown schematically in Figure 9d.

A third, wet etching step carried out on the remaining portions of the polysilicon layer 15 and a fourth etching step carried out on just the first thin dielectric layer 12' will complete the formation of the spacers 50, thereby exposing the base region 3 again, as shown in Figure 9e.

The HBT transistor formed according to the teachings of this invention can then be completed with conventional processes to form an emitter region 4 within the base region 2.

Finally, the emitter region 4 will be overlaid with a corresponding top emitter contact 9, optimized to enhance the injection efficiency of the HBT transistor.

Figure 9f is a comprehensive view showing the HBT transistor with a Ge_xSi_{1-x} heterojunction and the emitter contact 9 consisting of a first polysilicon layer 7, heavily doped with impurities of the N type and capped by a metal layer 8.

A first modification of the process for fabricating HBT transistors will now be described which falls within the protection scope of this Patent Application and comprises processing steps which are identical with those described above up to the moment of forming the first thin dielectric layer 12' of silicon dioxide.

In this embodiment, the first thin dielectric layer of silicon dioxide is replaced by a thick dielectric layer of silicon dioxide (SiO_2) also deposited by chemical vapor deposition (CVD).

In this embodiment, the thick dielectric layer of silicon dioxide could also be deposited by an APCVD process, followed by an optional thermal process.

The steps of the first modification of the fabrication process include: depositing a layer 14 of polysilicon; etching inside the window region; and forming an emitter region overlaid by an electric contact, similar to the first embodiment described.

Also within the principle of this invention, a second modification of the HBT transistor fabrication process will now be disclosed which includes the same process steps as those previously described up to the moment of forming the first thin dielectric layer 12'.

In this embodiment, the first thin dielectric layer 12' is formed by depositing a sacrificial silicon (Si) layer and then subjecting it to thermal oxidation. This sacrificial layer is deposited inside the window region 10 in direct contact with the Ge_xSi_{1-x} heterostructure included in the substrate 1.

Advantageously, the process steps described for forming the first thin dielectric layer 12' by a sacrificial layer will yield the same results, in terms of quality of the SiO_2/Ge_xSi_{1-x} interface, as were obtained previously by forming the layer 12' with a chemical vapor deposition (CVD) process.

It has been found that the sacrifical layer deposited inhibits the formation of the occluded germanium layer between the heterostructure and the first thin dielectric layer 12' because it prevents the oxidation process from reaching the $GexSi_{1-x}$ heterostructure.

In order to further minimize the surface re-combination phenomena that occur at the SiO_2/Ge_xSi_{1-x} interface, the second modification of the process may also have the step of forming the thin dielectric layer 12' followed by a suitable thermal treatment.

The steps of the second modification of the HBT transistor fabrication process will then include: depositing a second dielectric layer; depositing a layer 14 of polysilicon; etching inside the window region; and forming an emitter region overlaid by an electric contact, similar to the first embodiment described.

To improve the adhesion of the second dielectric layer 14 on the first thin dielectric layer 12', the second dielectric layer may comprise silicon nitride ($Si3N_4$).

Again within the principle of this invention, a third modification of the HBT transistor fabrication process is provided which includes processing steps identical with those previously described in relation to the second process modification up to the moment when the first thin dielectric layer 12' is formed.

In this embodiment, the first dielectric layer of silicon dioxide is further grown thermally to provide a dielectric layer of increased thickness embedding, or replacing, the second dielectric layer 14.

In order to minimize the surface re-combination phenomena that occur at the SiO_2/Ge_xSi_{1-x} interface, the third modification of the HBT transistor fabrication process may also have the oxidation step followed by a suitable thermal treatment.

The next steps of the third modification of the fabrication process will include: depositing a layer 15 of polysilicon; etching inside the window region; and forming an emitter region overlaid by an electric contact, similar to the second embodiment described.

Advantageously, by adopting the fabrication processes of this Patent Application, the technical problem of the base current deviating from the ideal in HBT transistors can be solved.

The truth of this statement is brought out by the graph in Figure 11 which illustrates the behavior of the collector (Ic) and base (IB) currents versus bias voltage (Vbe), as applied between the base and the emitter, for two HBT transistors having the same emitter surface area but formed with different fabrication methods. In fact, two patterns can be distinguished on this graph: the one (broken line) associated with the HBT transistor which has the layer 12 grown by thermal oxidation, and

the other (full line) associated with the HBT transistor formed by the process of this invention with the layer 12' deposited by CVD. These two patterns nearly match each other, and this match reveals a marked reduction in the deviation of the base current from the ideal.

Figure 12 shows, for the same types of HBT transistors as above, the behavior of their respective collector currents (Ic) versus the bias voltage (Vce) across the collector and emitter.

It is evinced from this graph that, for HBT transistors fabricated by the process of the invention (full line curve), a significant increase occurs in the variation percent of the current gain versus the collector current. It should be also emphasized that these transistors have low saturation voltage values, thereby affording lower power consumption.

Another advantage of this fabrication process or its first modification (CVD deposition of the layer 12') is that it involves relatively low deposition temperatures. This prevents back diffusion of the implanted acceptor impurities, thereby avoiding an oxidation-enhanced diffusion of B and further raising the cut-off frequency of the HBT transistor fabricated by the process of this invention.

A confirmation of the above statements can be found in the graphs of Figure 13 and Figure 14 which show, for the two types of HBT transistors described above, the concentration profile of the acceptor impurities versus depth into the substrate and the behavior of the cut-off frequency versus the collector bias current.

Finally, notice that collector bias currents in the milliAmpere range allow HBT transistors fabricated with the invention process to attain cut-off frequencies in the 20 GHz range, that is hitherto unattainable values.

In conclusion, the fabrication process of this invention allows the frequency field of application of HBT transistors to be further extended, while eliminating deviations of the base current from the ideal.

Claims

1. A process for fabricating a vertical structure high carrier mobility transistor on a substrate (1) of crystalline silicon doped with impurities of the N type, having a collector region (2) located at a lower portion of the substrate, the process comprising the steps of:

- defining a window (10) in the semiconductor substrate (1);
- providing a first implantation of germanium (Ge) atoms through said window;
- providing a second implantation of acceptor dopants through said window to define a base region (3);
- applying an RTA treatment, or treatment in an oven, to re-construct the crystal lattice within the semiconductor substrate comprising a silicon/germanium alloy (Si1-xGex);

characterized by the steps of:

- forming a first thin dielectric layer (12') of silicon dioxide (SiO_2) by chemical vapor deposition (CVD);
- depositing a second dielectric layer (14) onto said first dielectric layer (12');
- depositing a polysilicon layer (15) onto said second dielectric layer (14);
- etching away, within the window region (10), said first (12') and second (14) dielectric layers, and the polysilicon layer (15), to expose the base region and form isolation spacers (50) at the window edges;
- forming an N-doped emitter (4) in the base (3) and window regions.

2. A process according to Claim 1, characterized in that the deposition of the first thin dielectric layer (12') of silicon dioxide (SiO_2) is carried out by an atmospheric pressure chemical vapor deposition (APCVD) process.

3. A process according to Claim 1, characterized in that the deposition of the first thin dielectric layer (12') of silicon dioxide (SiO_2) is followed by thermal treatment.

4. A process according to Claim 1, characterized in that the second dielectric layer (14) is silicon nitride (Si_3N_4).

5. A process for fabricating a vertical structure high carrier mobility transistor on a substrate of crystalline silicon doped with impurities of the N type, having a collector region located at a lower portion of the substrate, the process comprising the steps of:

- defining a window in the semiconductor substrate;
- providing a first implantation of germanium (Ge) atoms through said window;
- providing a second implantation of acceptor dopants through said window to define a base region;
- applying an RTA treatment to reconstruct the crystal lattice within the semiconductor substrate comprising a silicon/germanium alloy

($Si_{1-x}Ge_x$);
characterized by the steps of:

- forming a thick dielectric layer of silicon dioxide (SiO_2) by chemical vapor deposition;
- depositing a polysilicon layer onto said dielectric layer;
- etching away, within the window region, said dielectric layer and the polysilicon layer to expose the base region and form isolation spacers at the window edges;
- forming an N-doped emitter in the base and window regions.

6. A process according to Claim 5, characterized in that the deposition of the thick dielectric layer of silicon dioxide (SiO_2) is carried out by an atmospheric pressure chemical vapor deposition (APCVD) process.

7. A process according to Claim 5, characterized in that the deposition of the thick dielectric layer of silicon dioxide (SiO_2) is followed by thermal treatment.

8. A process for fabricating a vertical structure high carrier mobility transistor on a substrate of crystalline silicon doped with impurities of the N type, having a collector region located at a lower portion of the substrate, the process comprising the steps of:

- defining a window in the semiconductor substrate; providing a first implantation of germanium (Ge) atoms through said window;
- providing a second implantation of acceptor dopants through said window to define a base region; applying an RTA treatment, or treatment in an oven, to re-construct the crystal lattice within the semiconductor substrate comprising a silicon/germanium alloy ($Si_{1-x}Ge_x$);
characterized by the steps of:
- forming a first thin dielectric layer of silicon dioxide (SiO_2) by deposition of a sacrificial silicon (Si) layer, subsequently subjected to a thermal oxidation step;
- depositing a second dielectric layer onto said first dielectric layer;
- depositing a polysilicon layer onto said second dielectric layer;
- etching away, within the window region, said first and second dielectric layers and the polysilicon layer to expose the base region and form isolation spacers at the window edges;
- forming an N-doped emitter in the base and window regions.

9. A process according to Claim 8, characterized in that the formation of the first thin dielectric layer of silicon dioxide (SiO_2) is followed by thermal treatment.

10. A process according to Claim 8, characterized in that the second dielectric layer is silicon nitride (Si_3N_4).

11. A process for fabricating a vertical structure high carrier mobility transistor on a substrate of crystalline silicon doped with impurities of the N type, having a collector region located at a lower portion of the substrate, the process comprising the steps of:

- defining a window in the semiconductor substrate; providing a first implantation of germanium (Ge) atoms through said window;
- providing a second implantation of acceptor dopants through said window to define a base region; applying an RTA treatment to re-construct the crystal lattice within the semiconductor substrate comprising a silicon/germanium alloy ($Si_{1-x}Ge_x$);
characterized by the steps of:
- forming a thick dielectric layer of silicon dioxide (SiO_2) by deposition of a sacrificial silicon (Si) layer, subsequently subjected to a thermal oxidation step;
- depositing a polysilicon layer onto said dielectric layer;
- etching away, within the window region, said dielectric layer and the polysilicon layer to expose the base region and form isolation spacers at the window edges;
- forming an N-doped emitter in the base and window regions.

12. A process according to Claim 12, characterized in that the formation of the thick dielectric layer of silicon dioxide (SiO_2) is followed by thermal treatment.

13. A vertical structure high carrier mobility bipolar transistor as obtained by the fabrication process according to Claim 1.

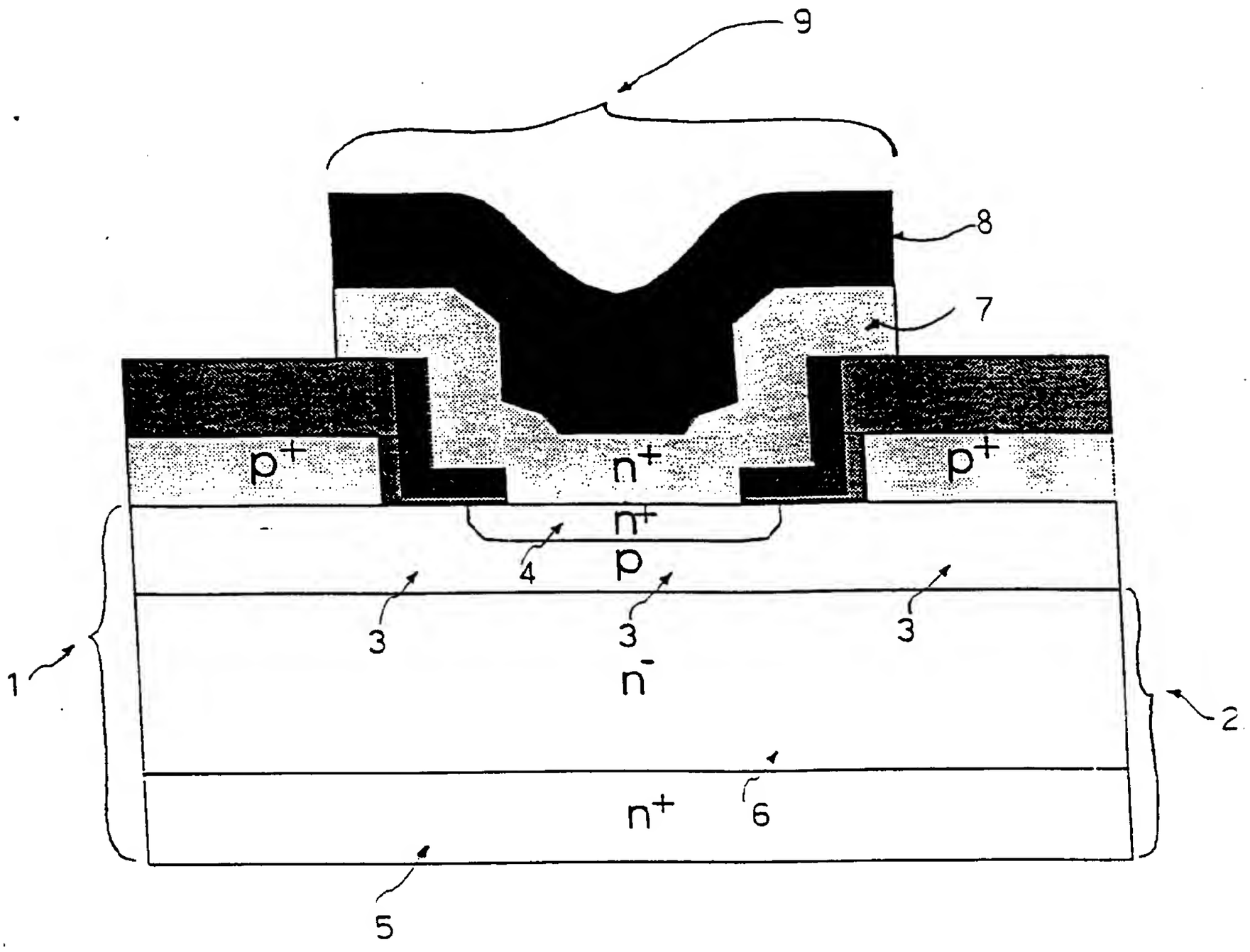
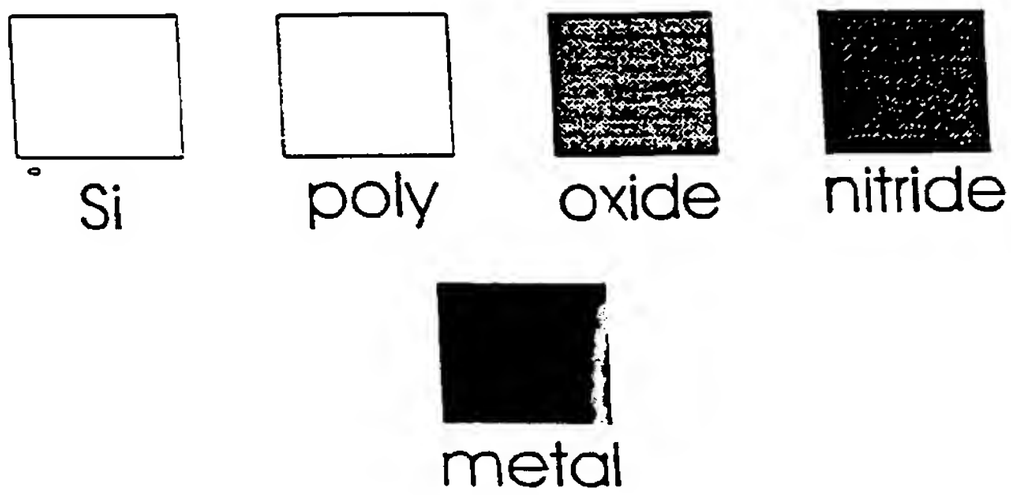


FIGURE 1



PRIOR ART

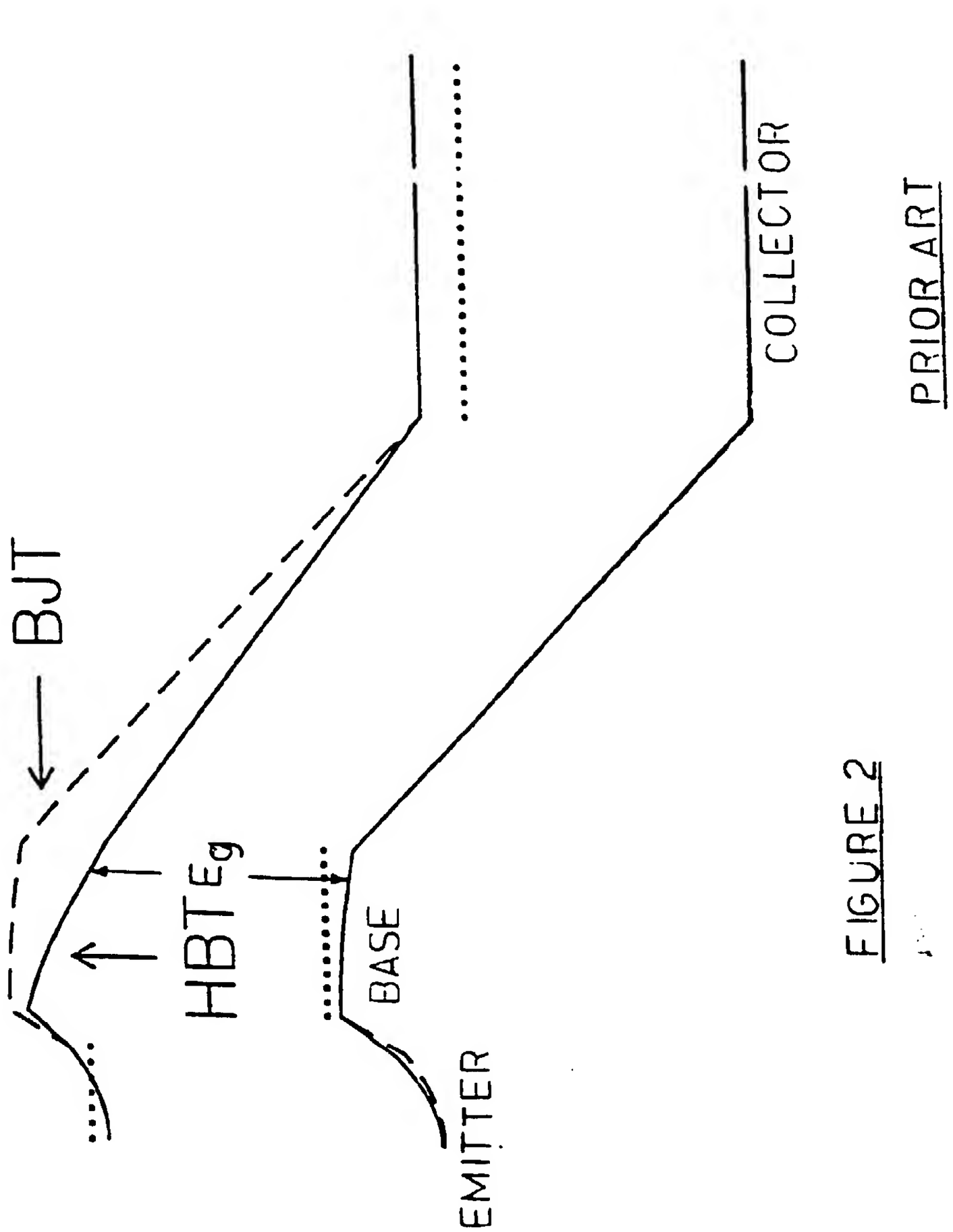
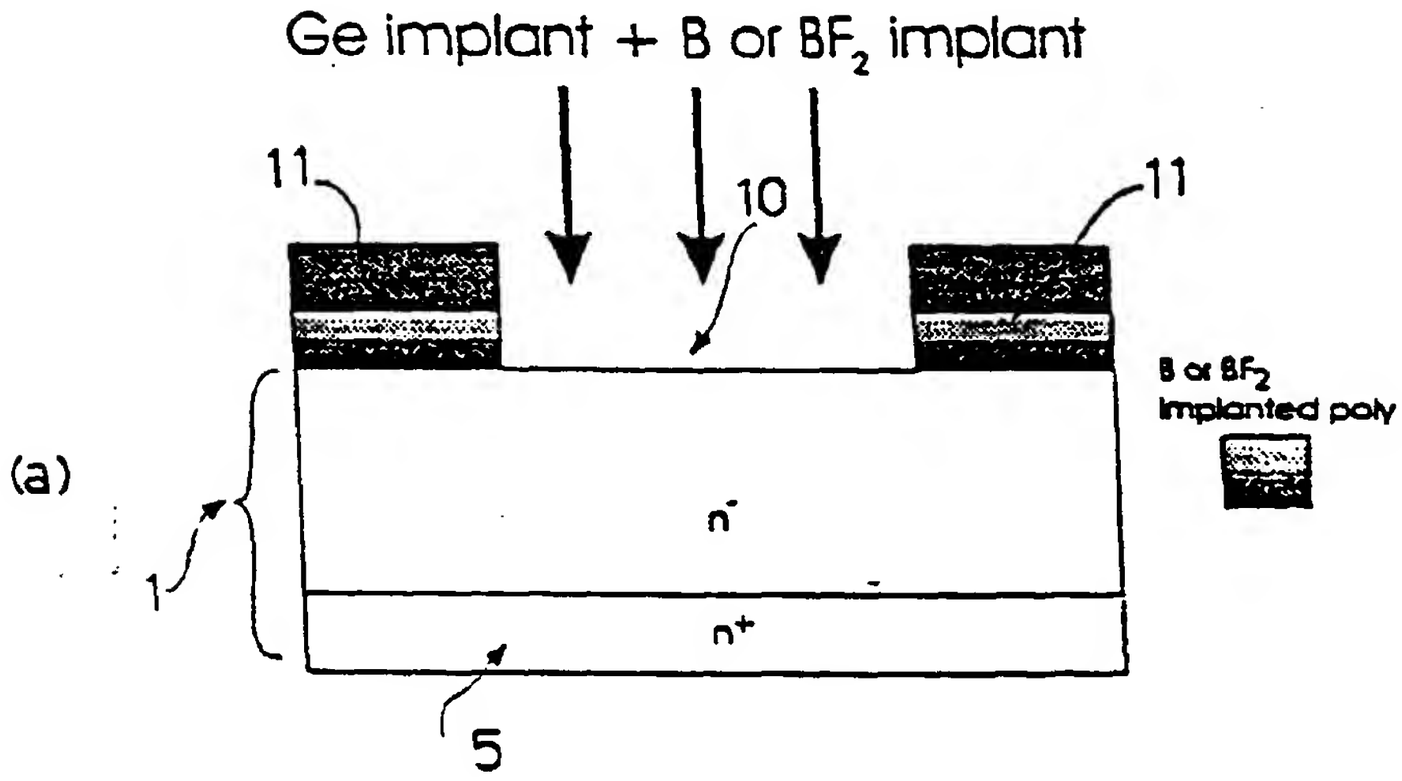


FIGURE 2

PRIOR ART

PRIOR ART



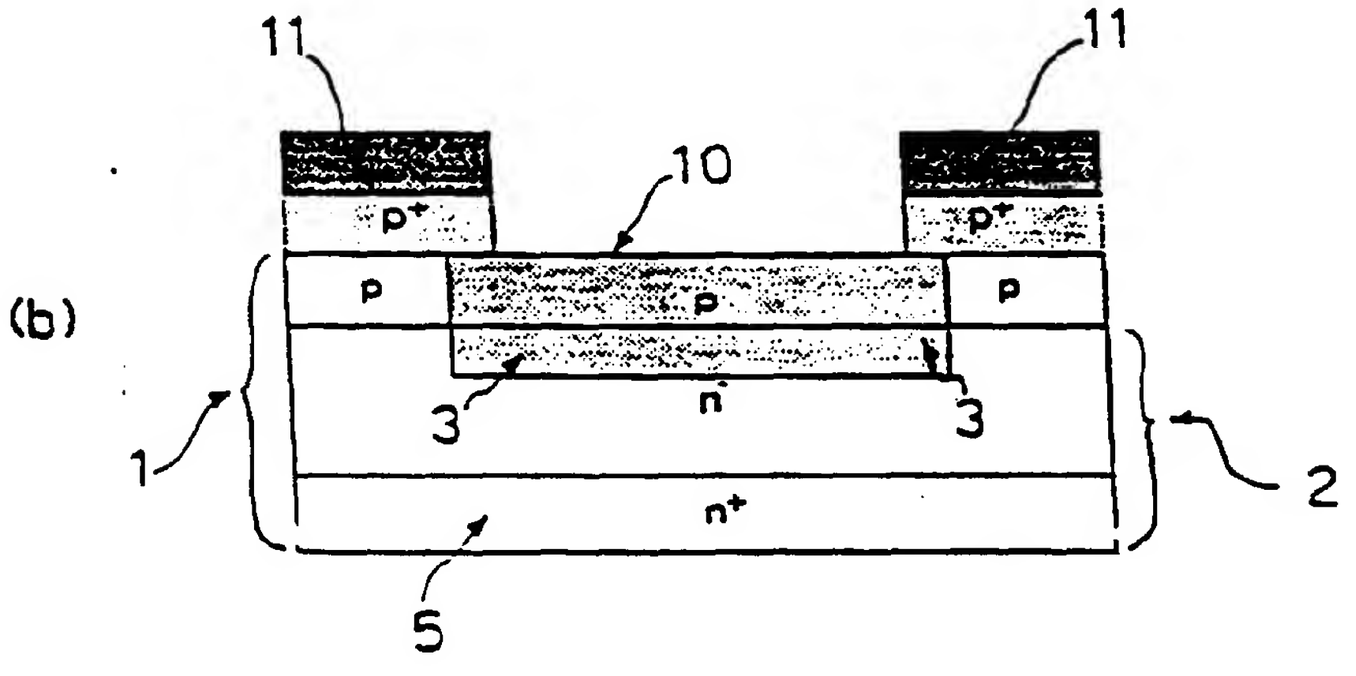
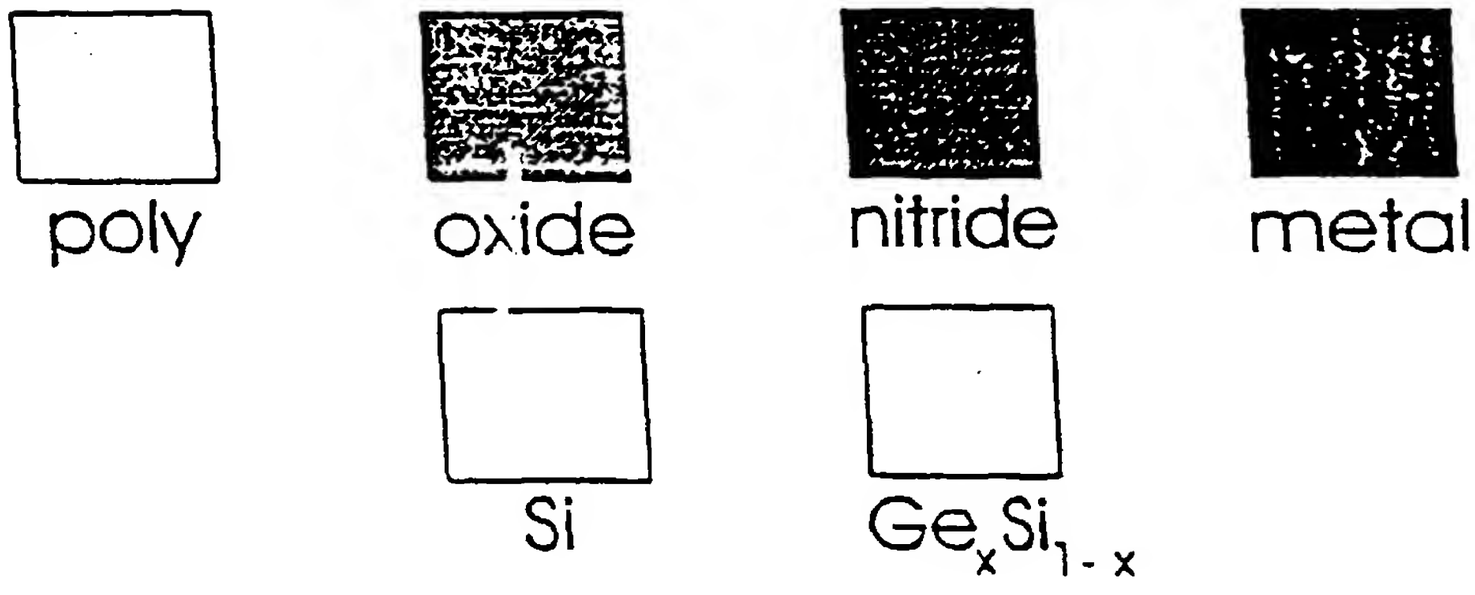
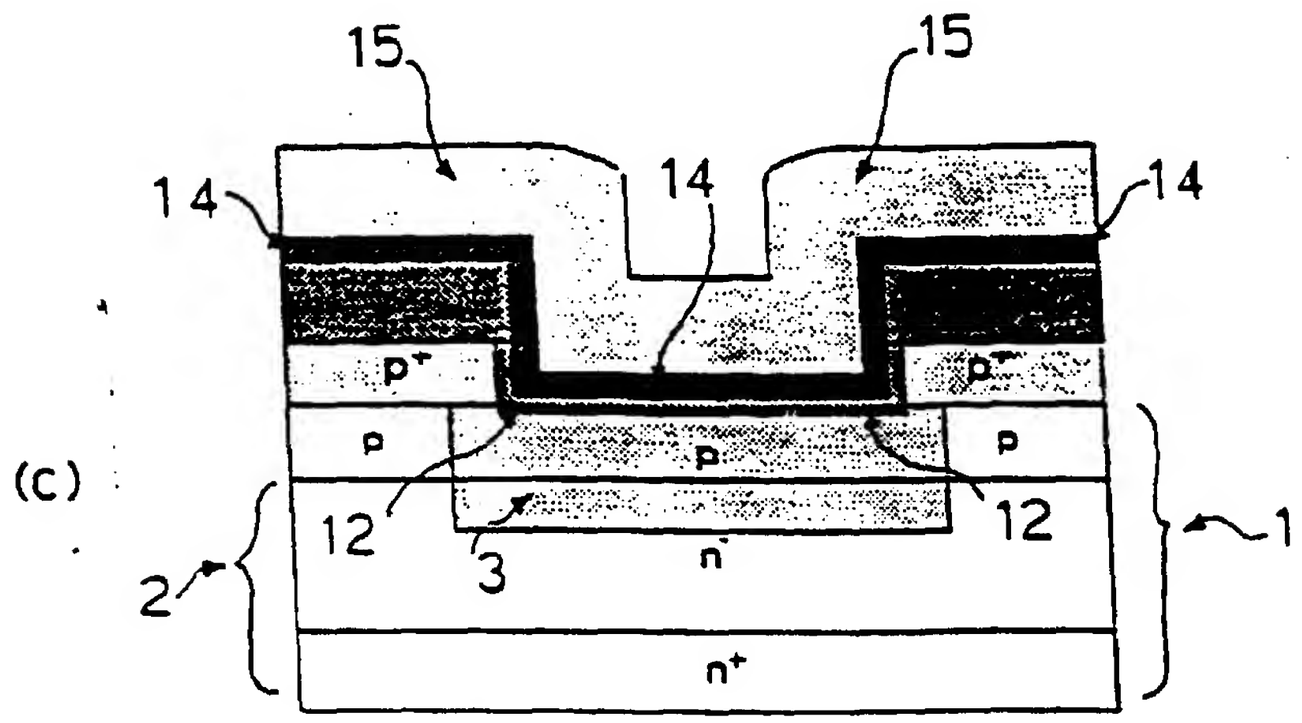


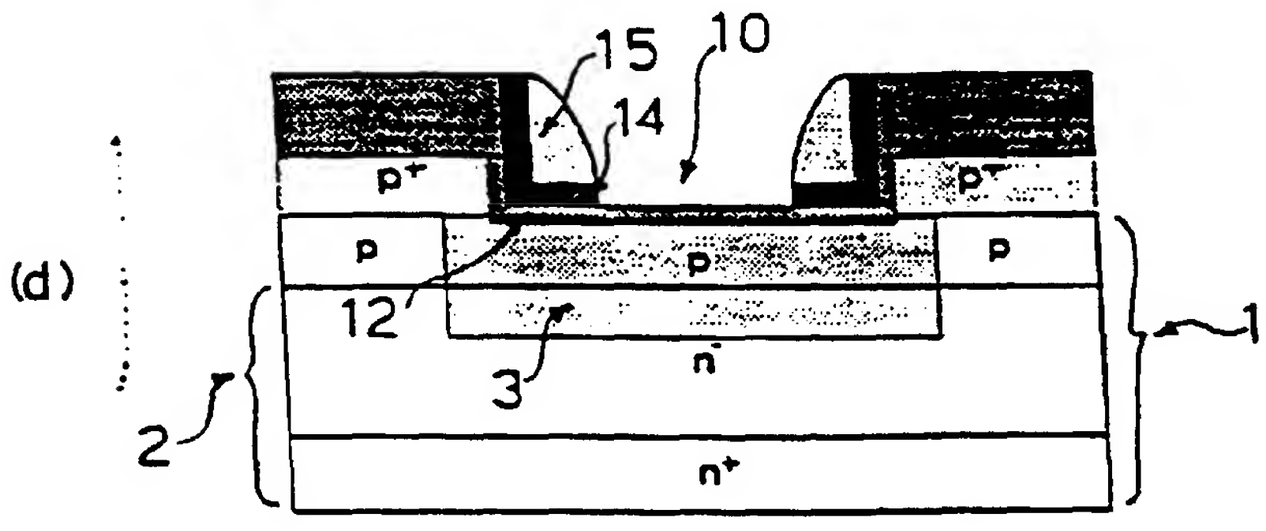
FIGURE 3



PRIOR ART



(c)



(d)

FIGURE 3

poly

oxide

nitride

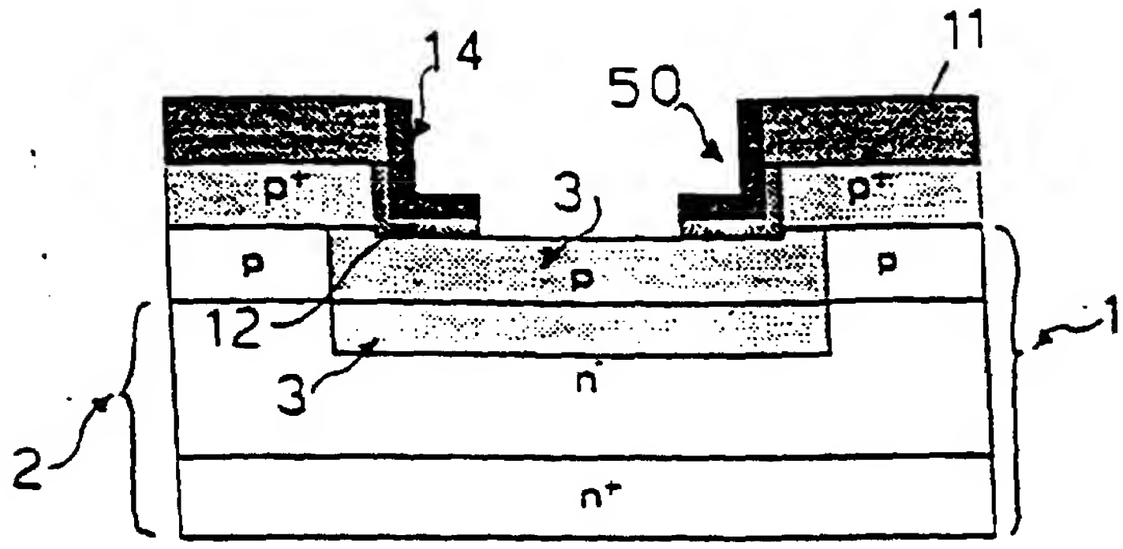
metal

Si

Ge_xSi_{1-x}

PRIOR ART

(e)



(f)

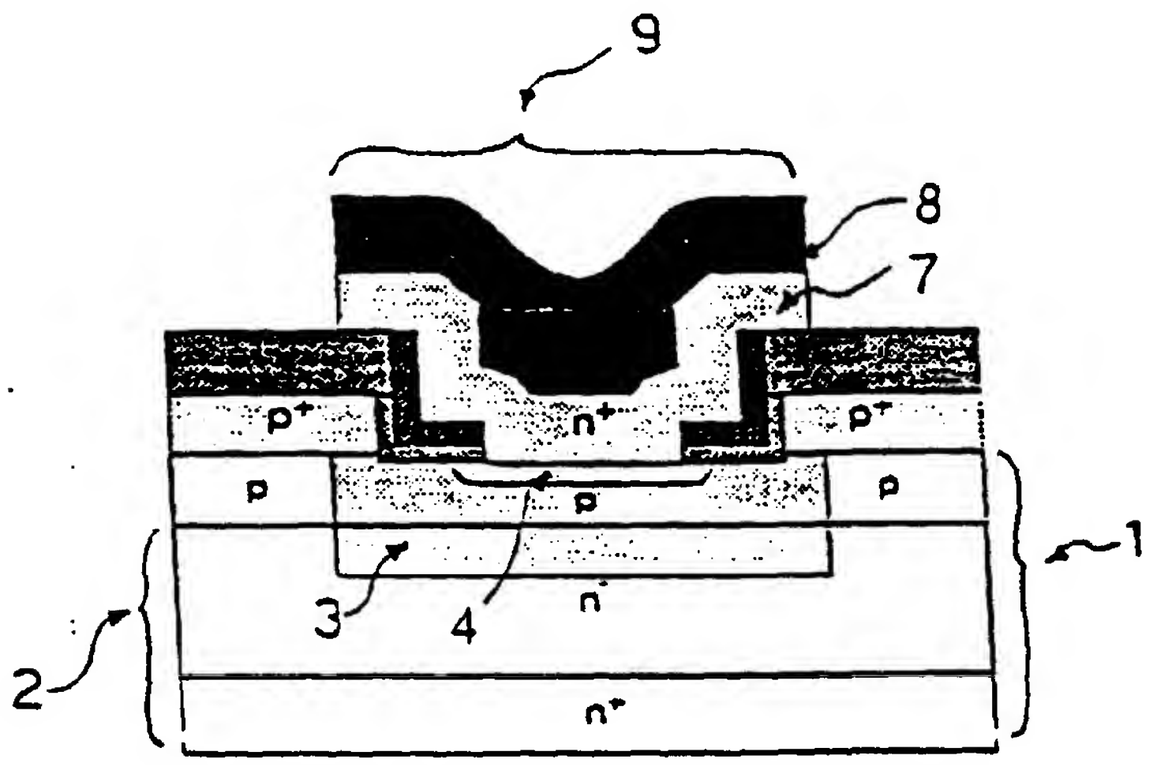


FIGURE 3

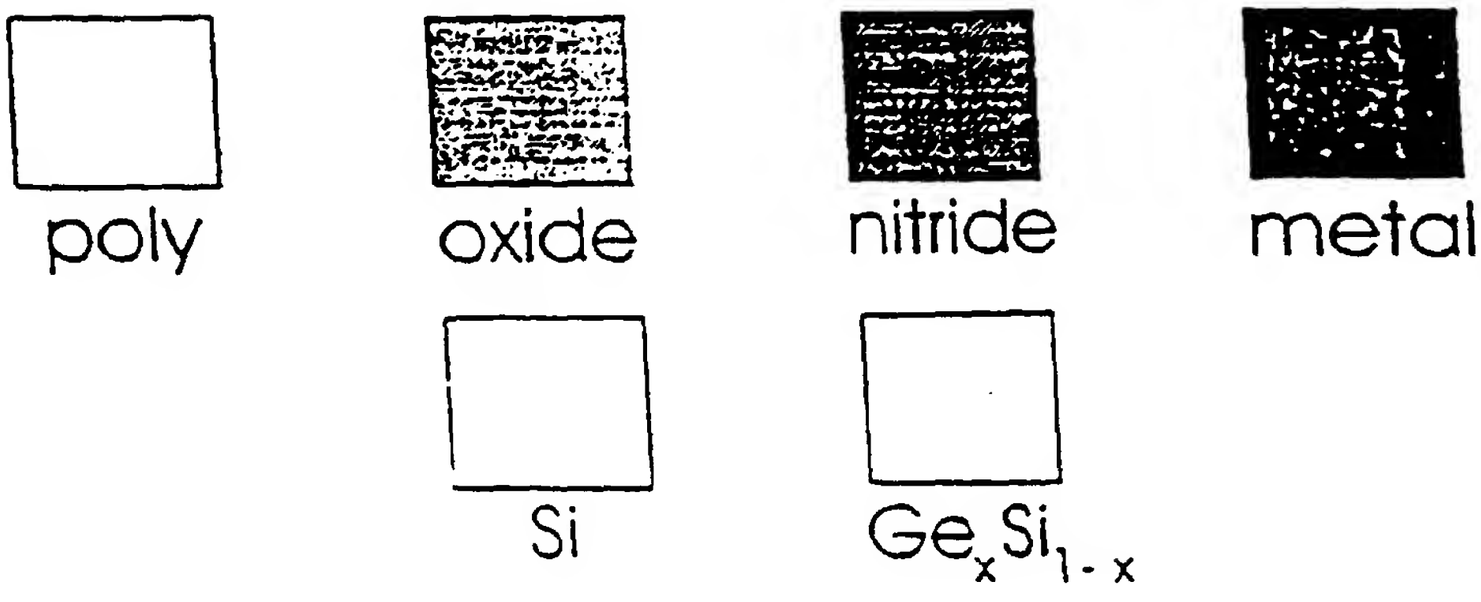
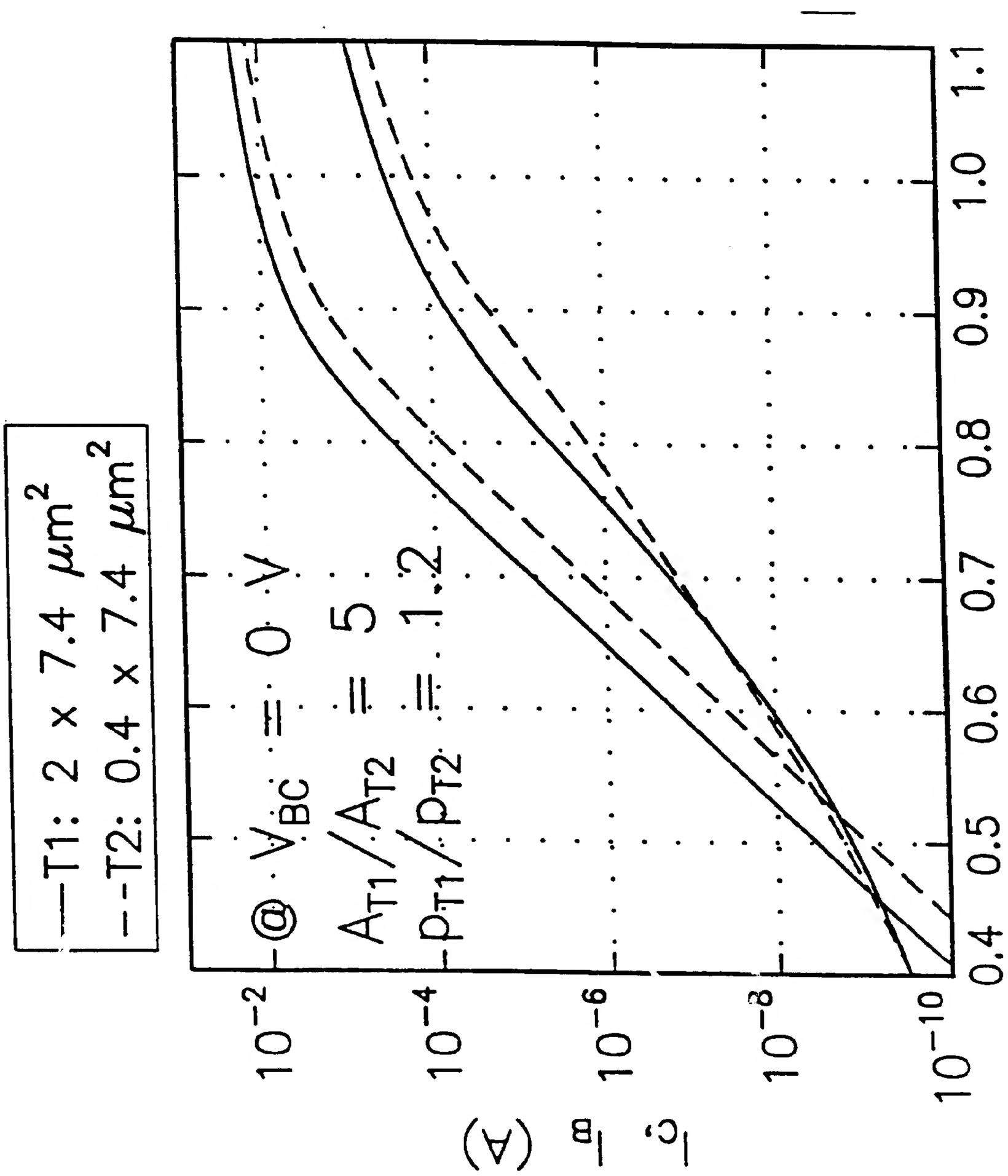


FIGURE 4


—T1: 2 x 7.4 μm²
--T2: 0.4 x 7.4 μm²
@ V_{BC} = 0 V
A_{T1} / A_{T2} = 5
p_{T1} / p_{T2} = 1.2
I_C, I_B (A)
10^{-2}
10^{-4}
10^{-6}
10^{-8}
10^{-10}
0.4
0.5
0.6
0.7
0.8
0.9
1.0
1.1
V_{BE} (V)

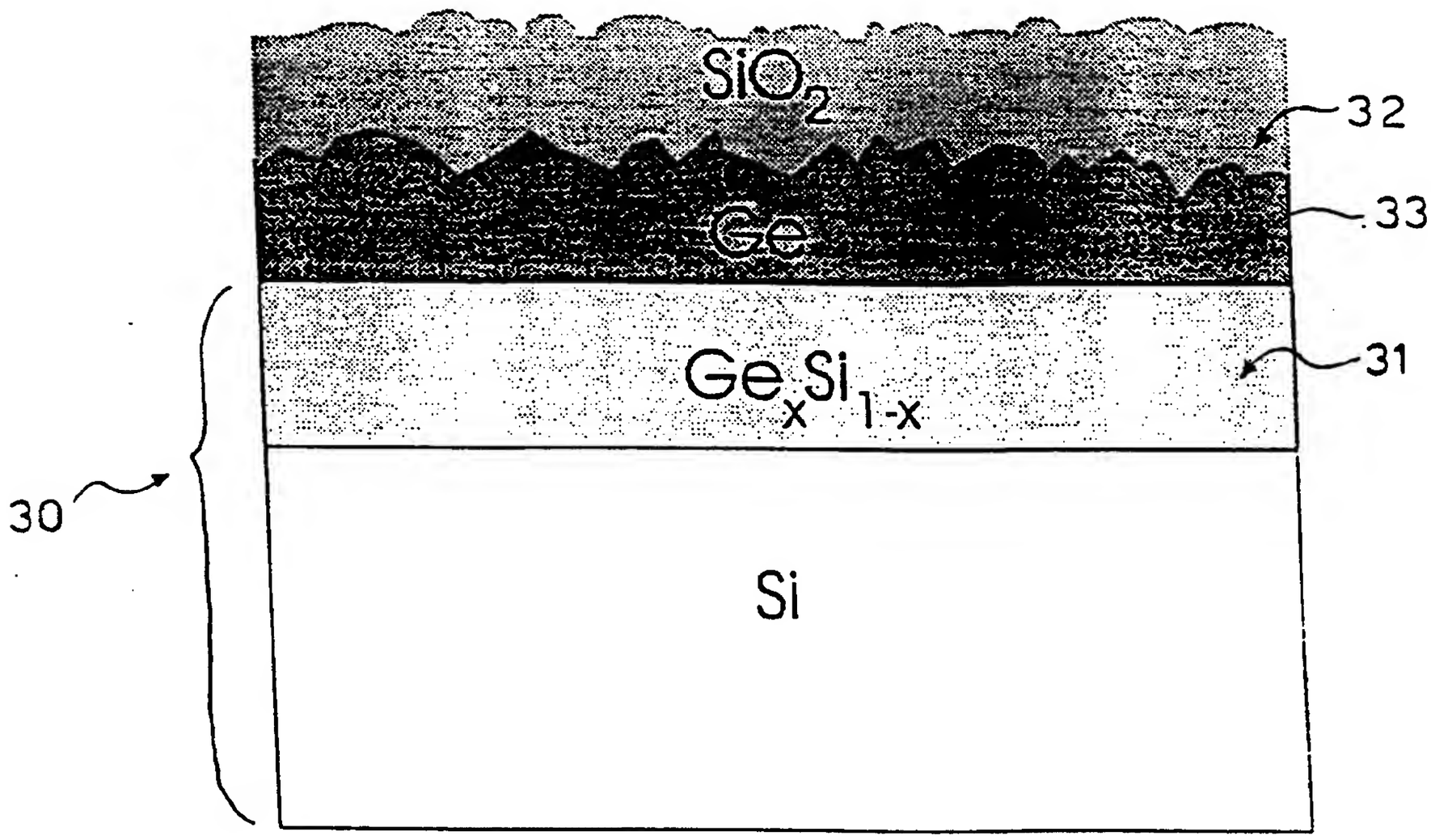
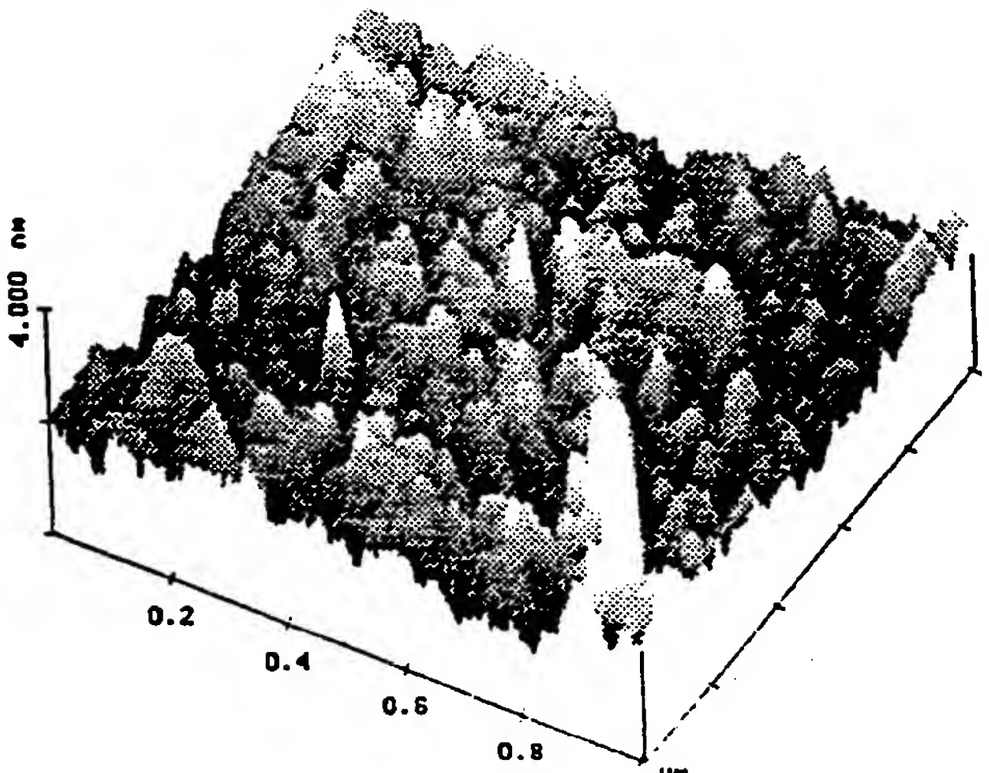


FIGURE 5



Thermal oxide in Ge_xSi_{1-x}

FIGURE 6

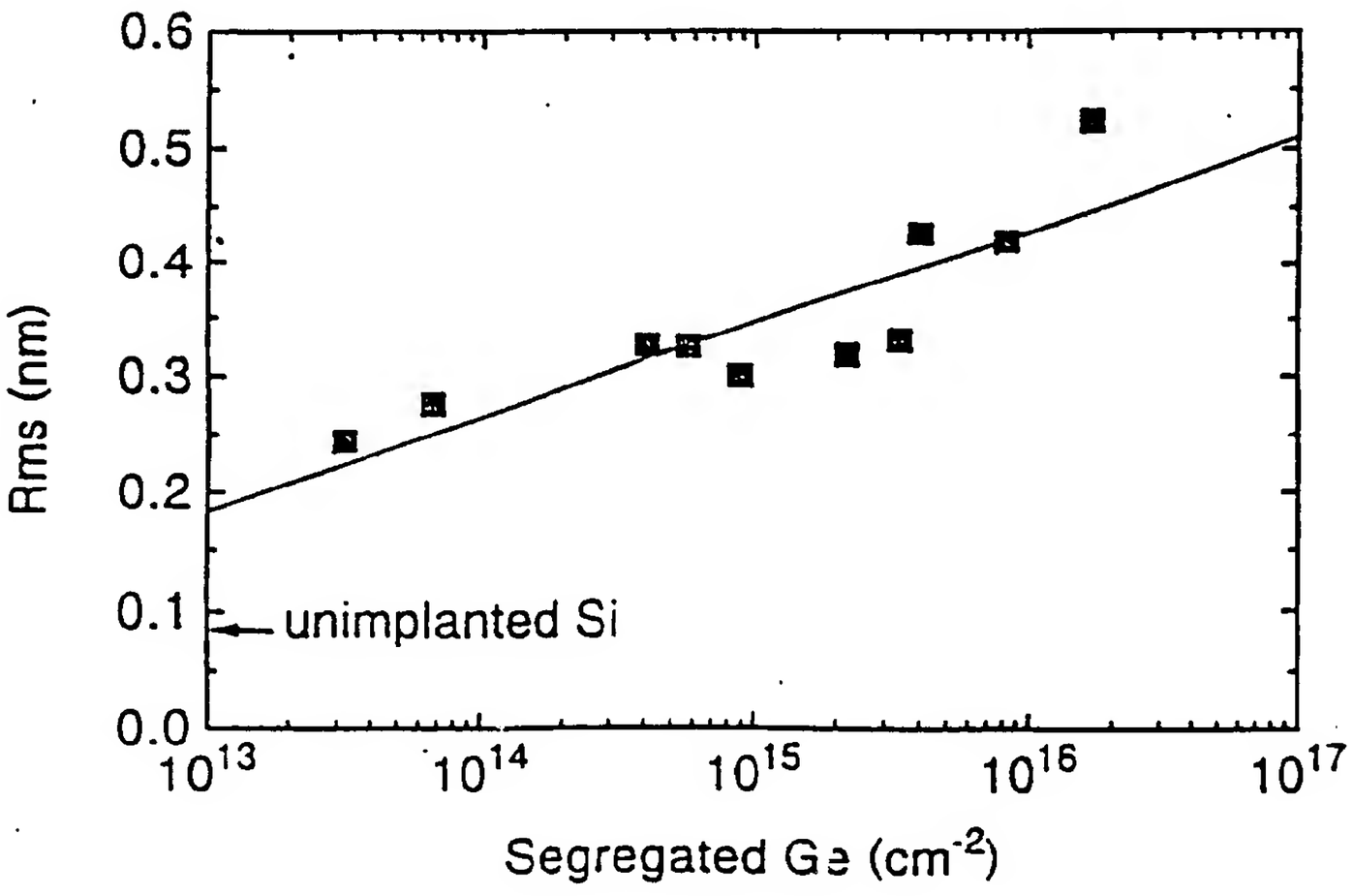


FIGURE 7

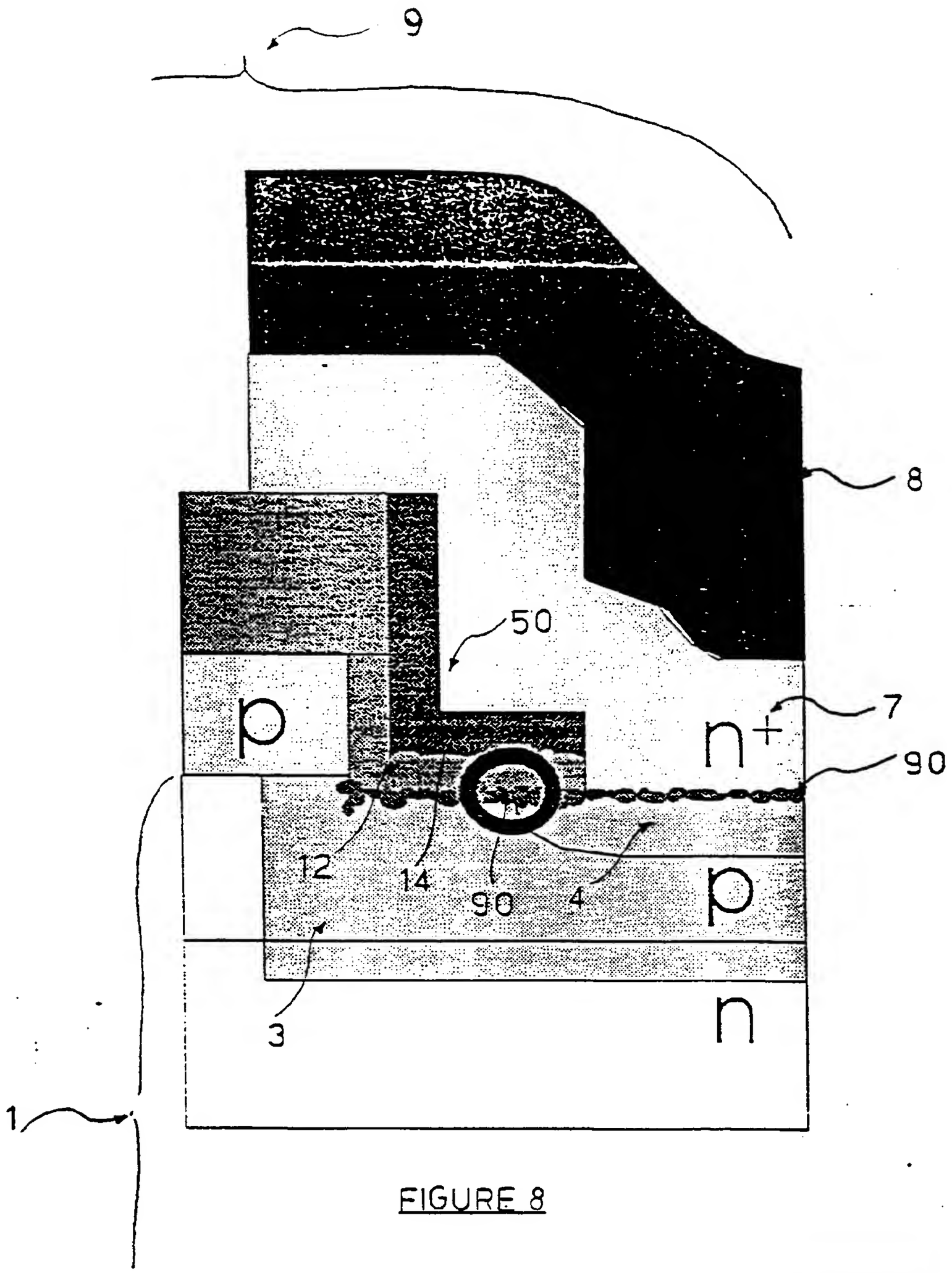

9
8
50
p
n+
7
90
12
14
90
4
p
3
n
1
poly
oxide
nitride
metal
Si
Ge x Si 1 - x
Ge

FIGURE 8

INVENTION

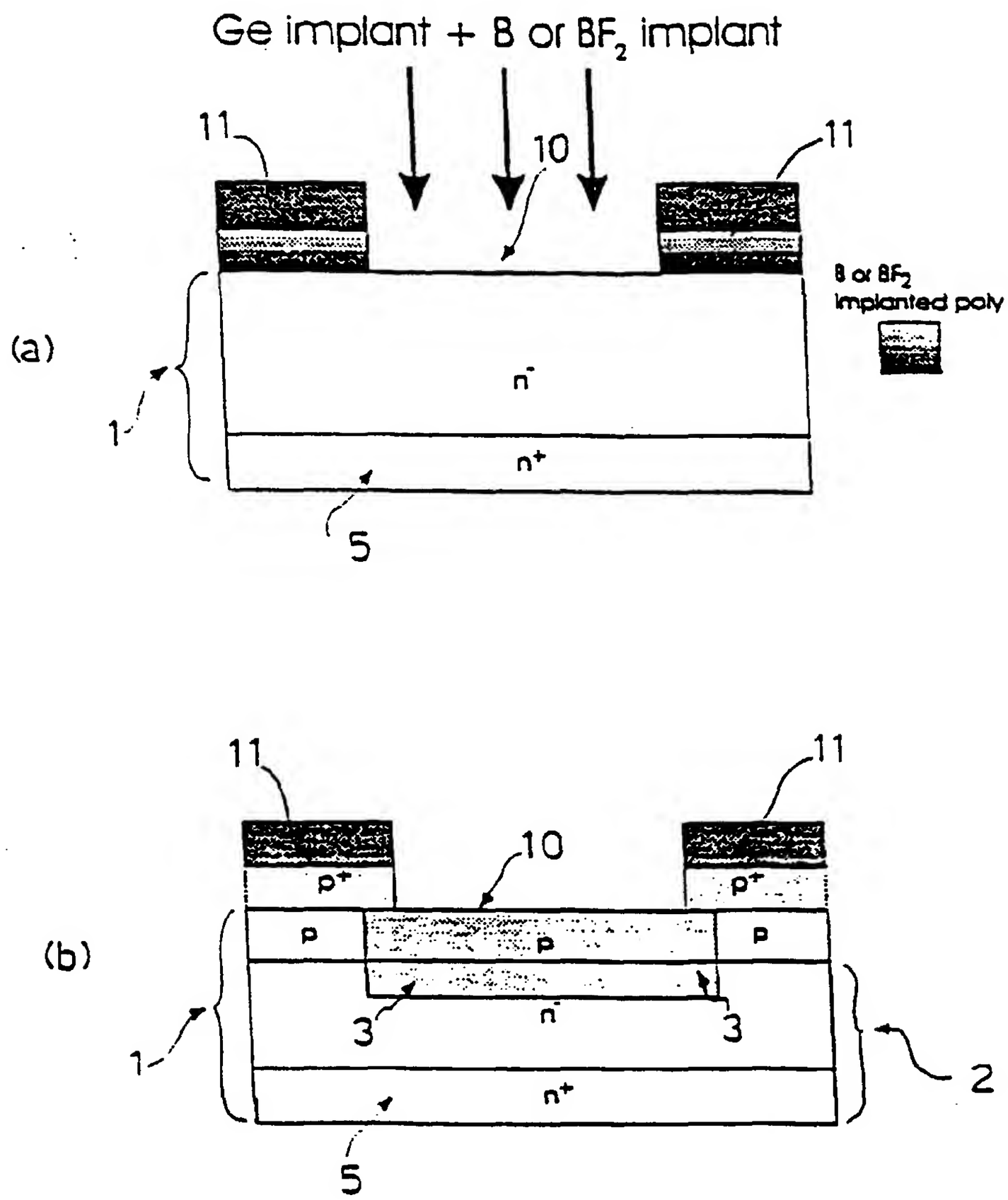
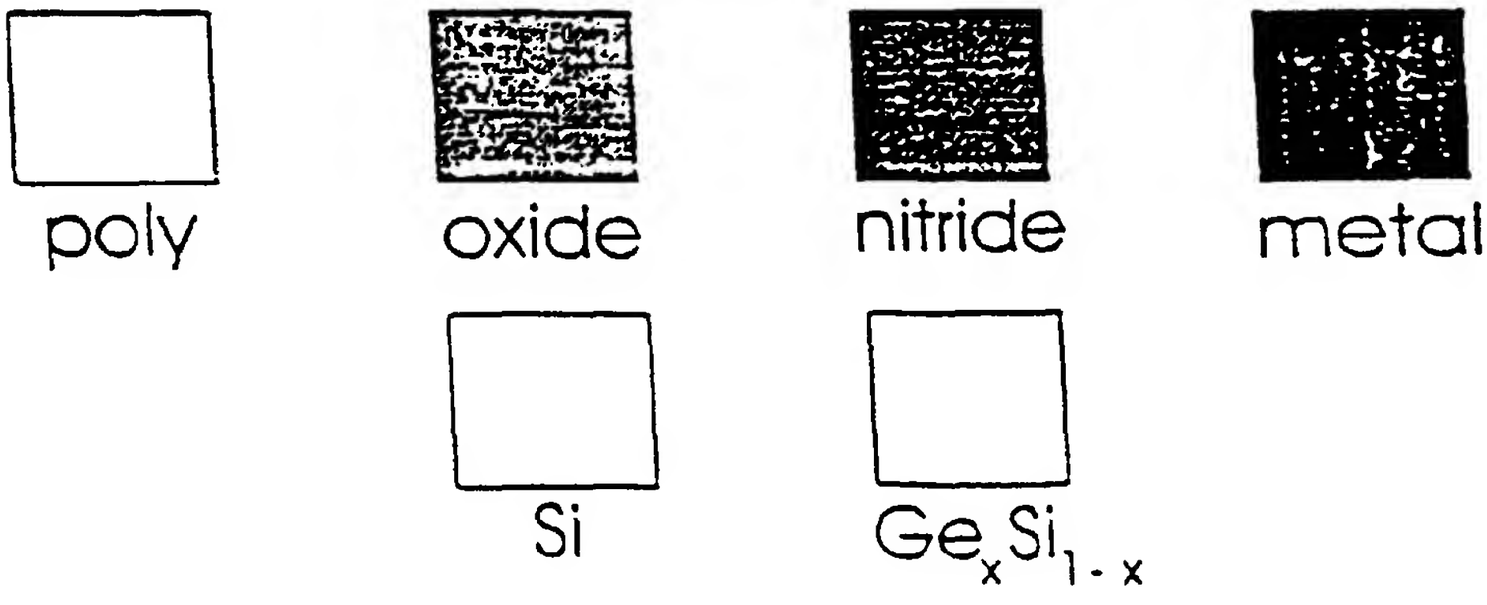
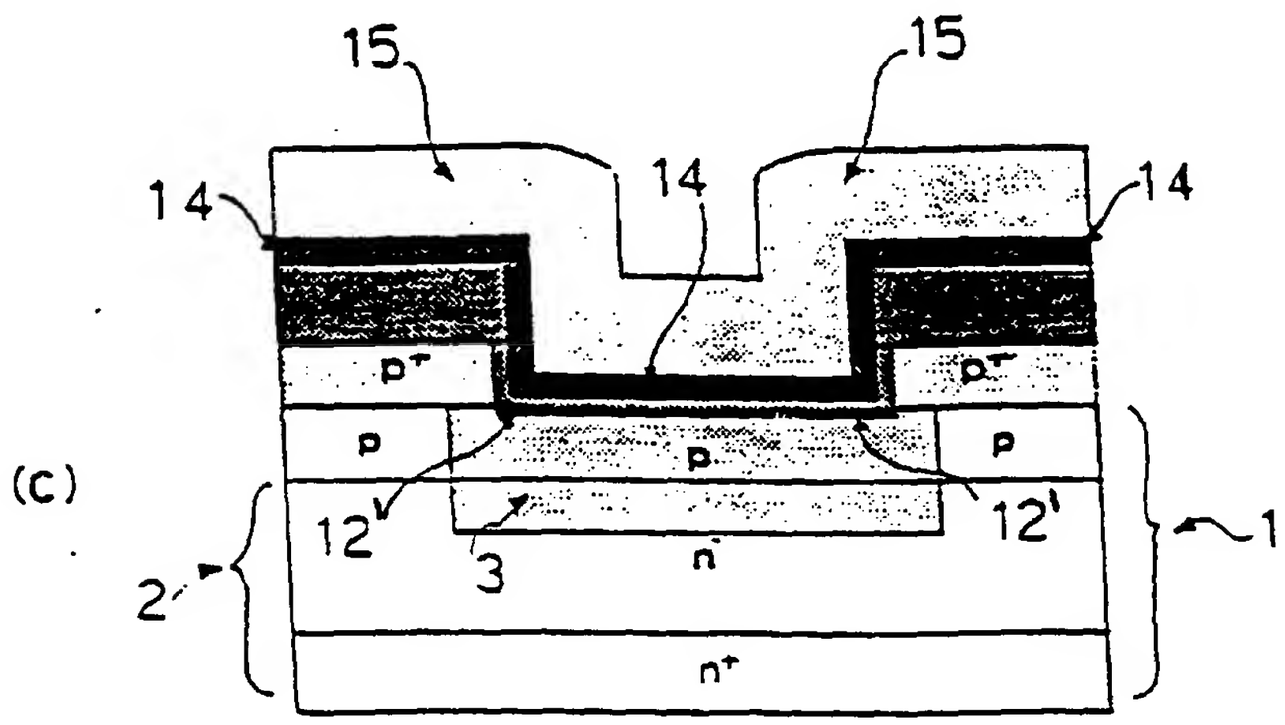


FIGURE 9



INVENTION



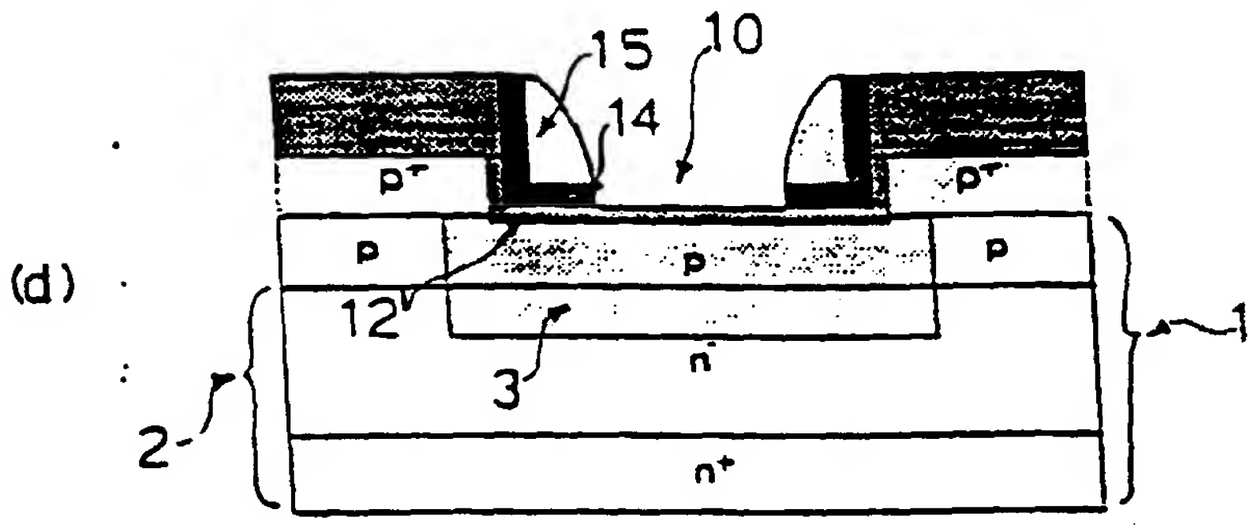
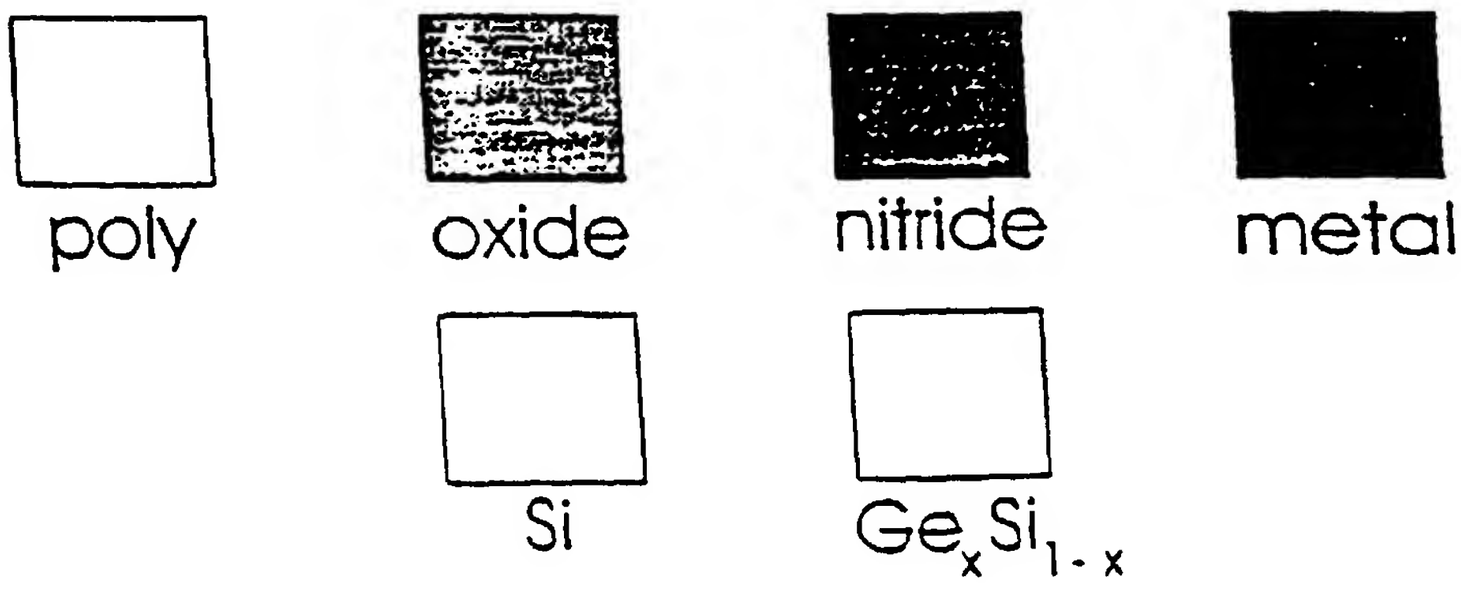
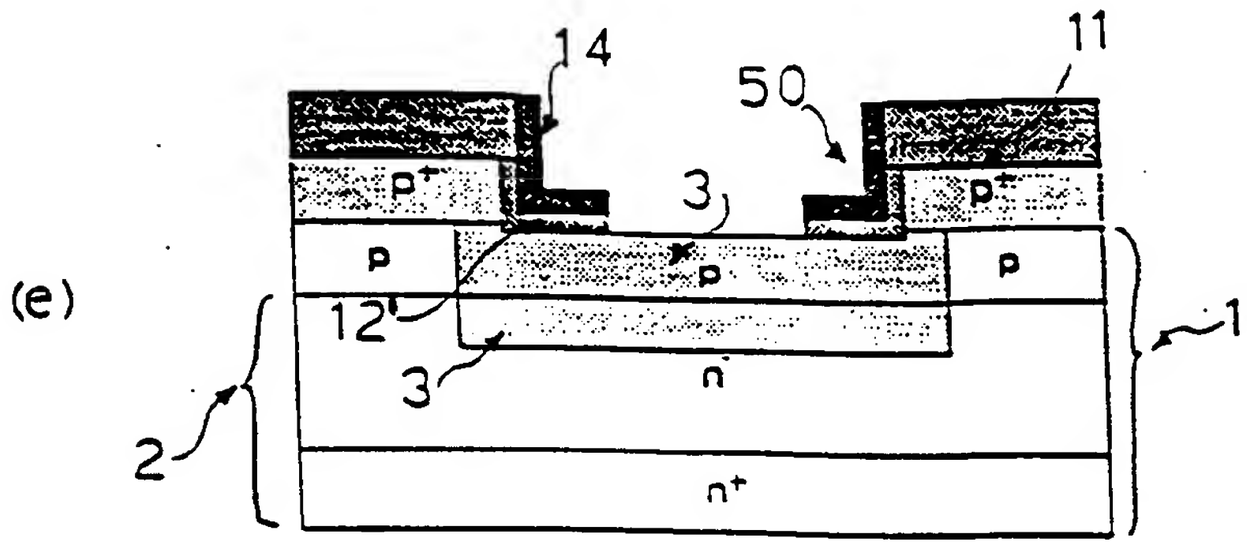


FIGURE 9



INVENTION



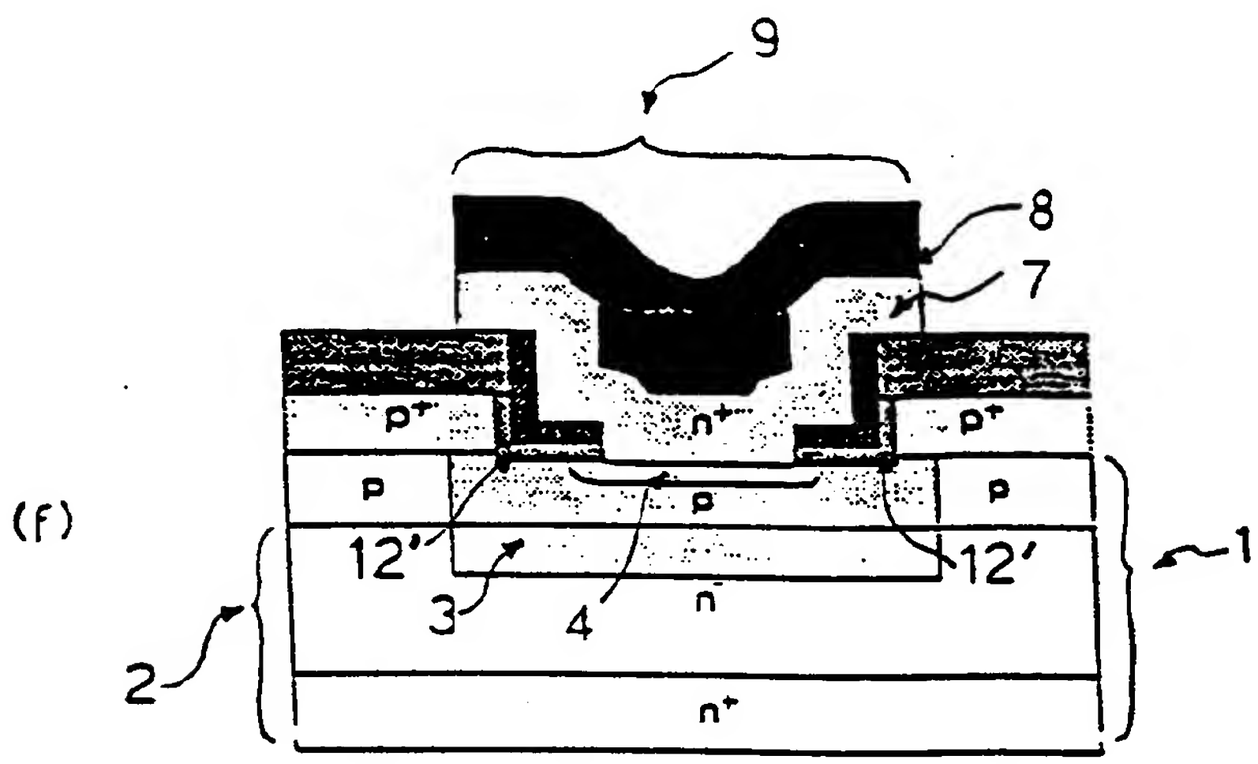


FIGURE 9

poly

oxide

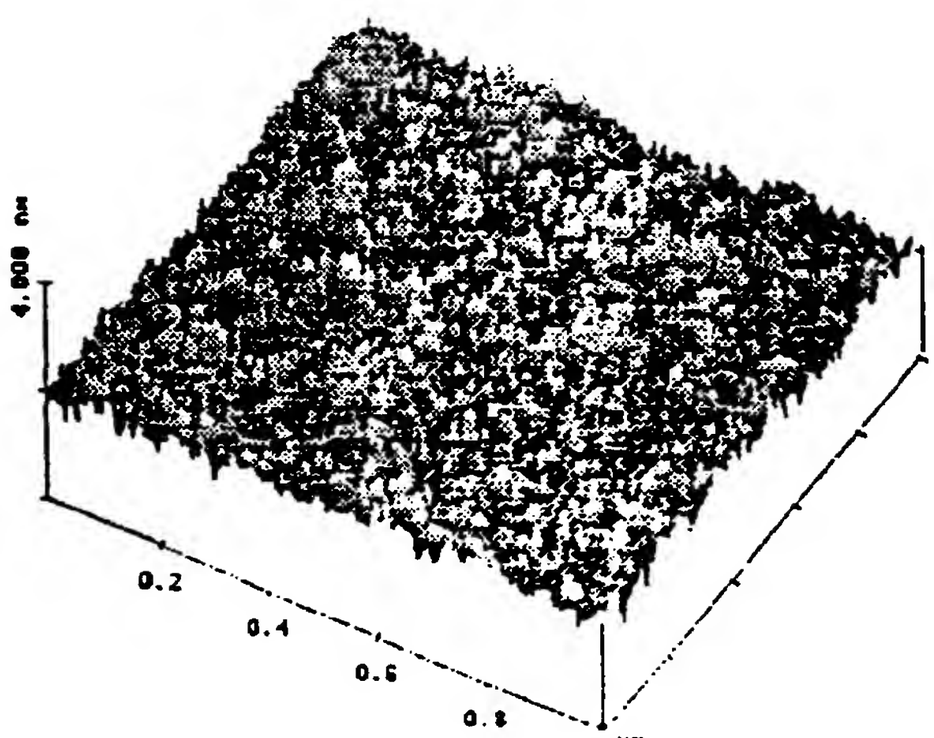
nitride

metal

Si

Ge_xSi_{1-x}

INVENTION



CVD oxide in Ge_xSi_{1-x}

FIGURE 10

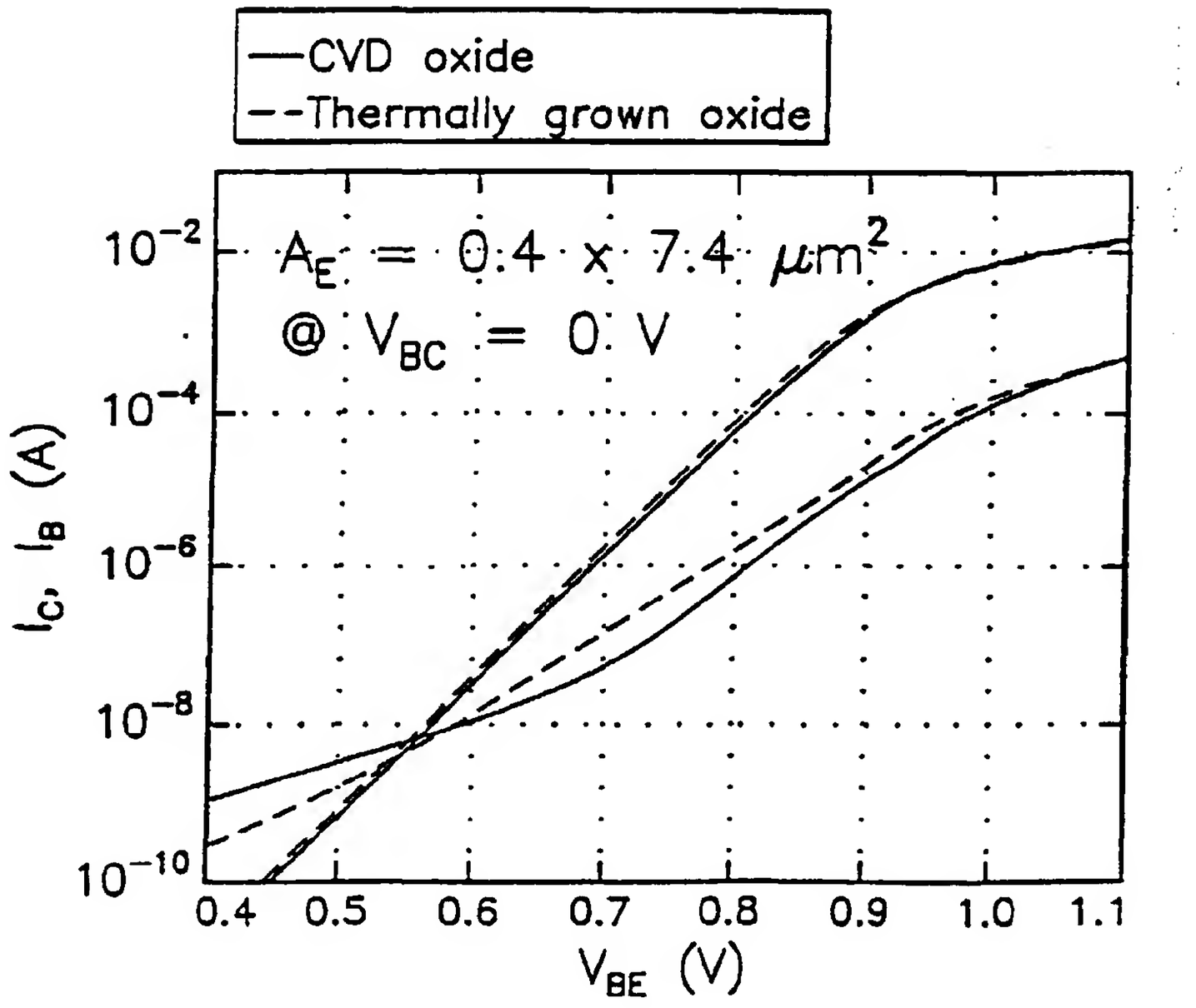


FIGURE 11

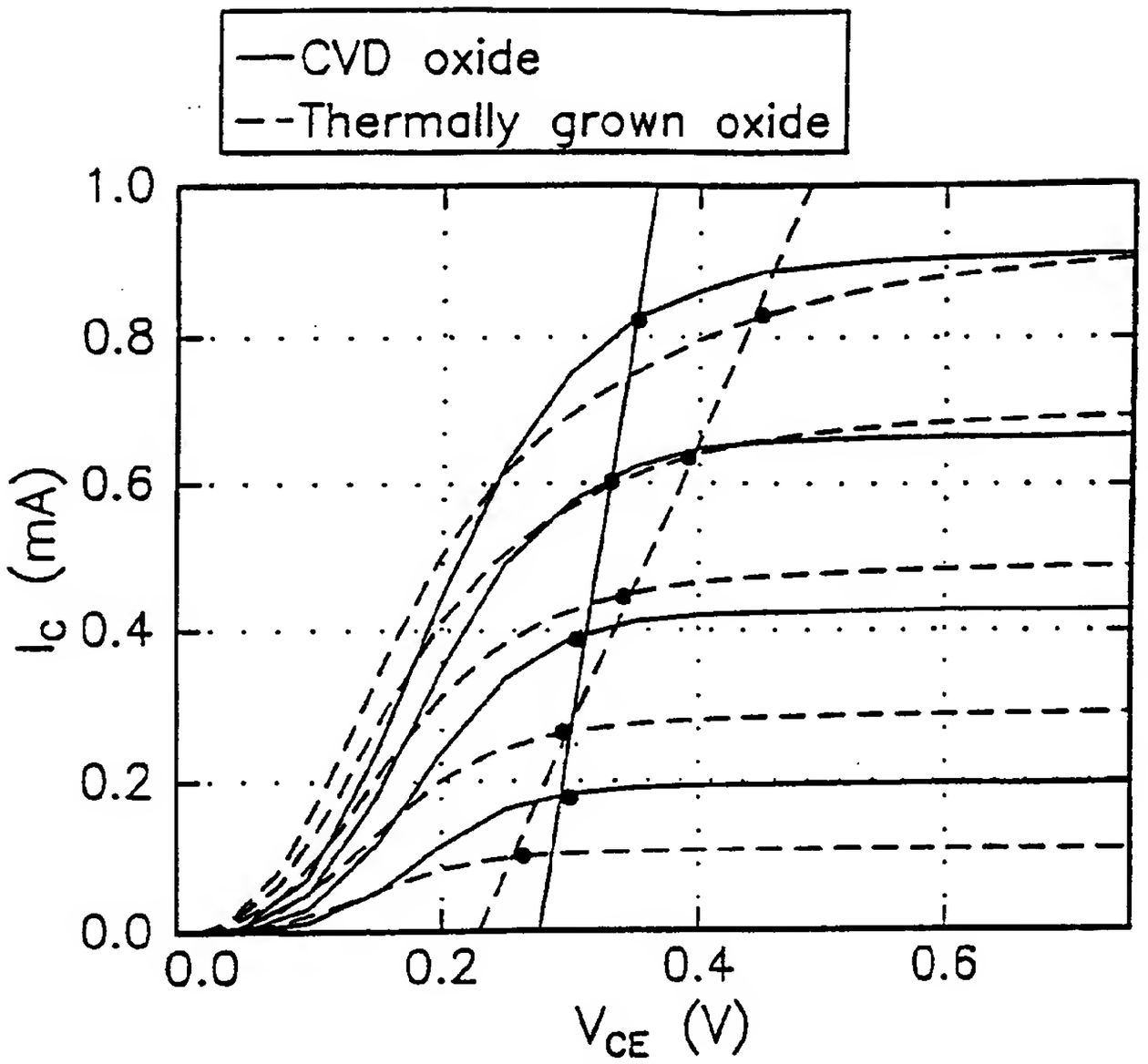


FIGURE 12

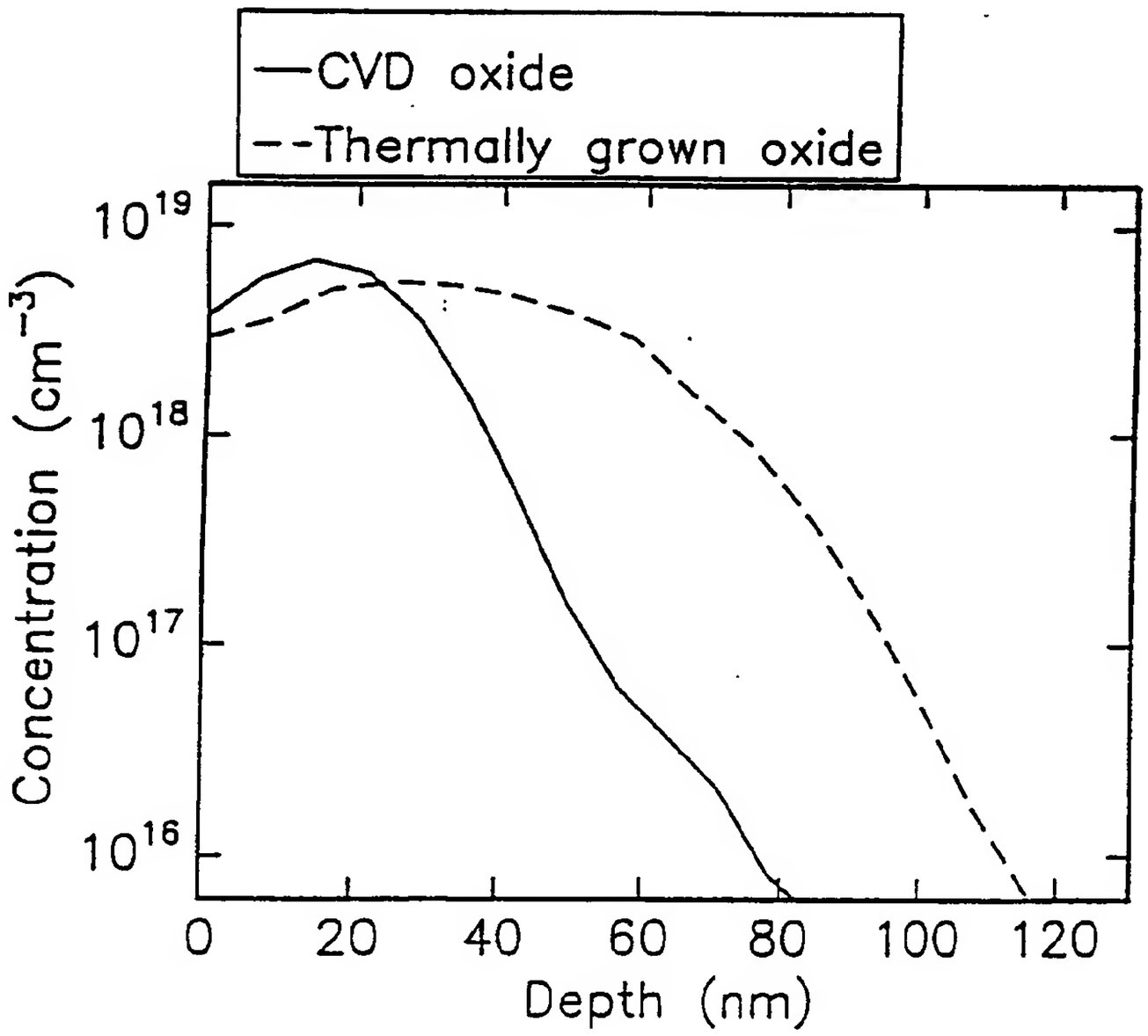


FIGURE 13

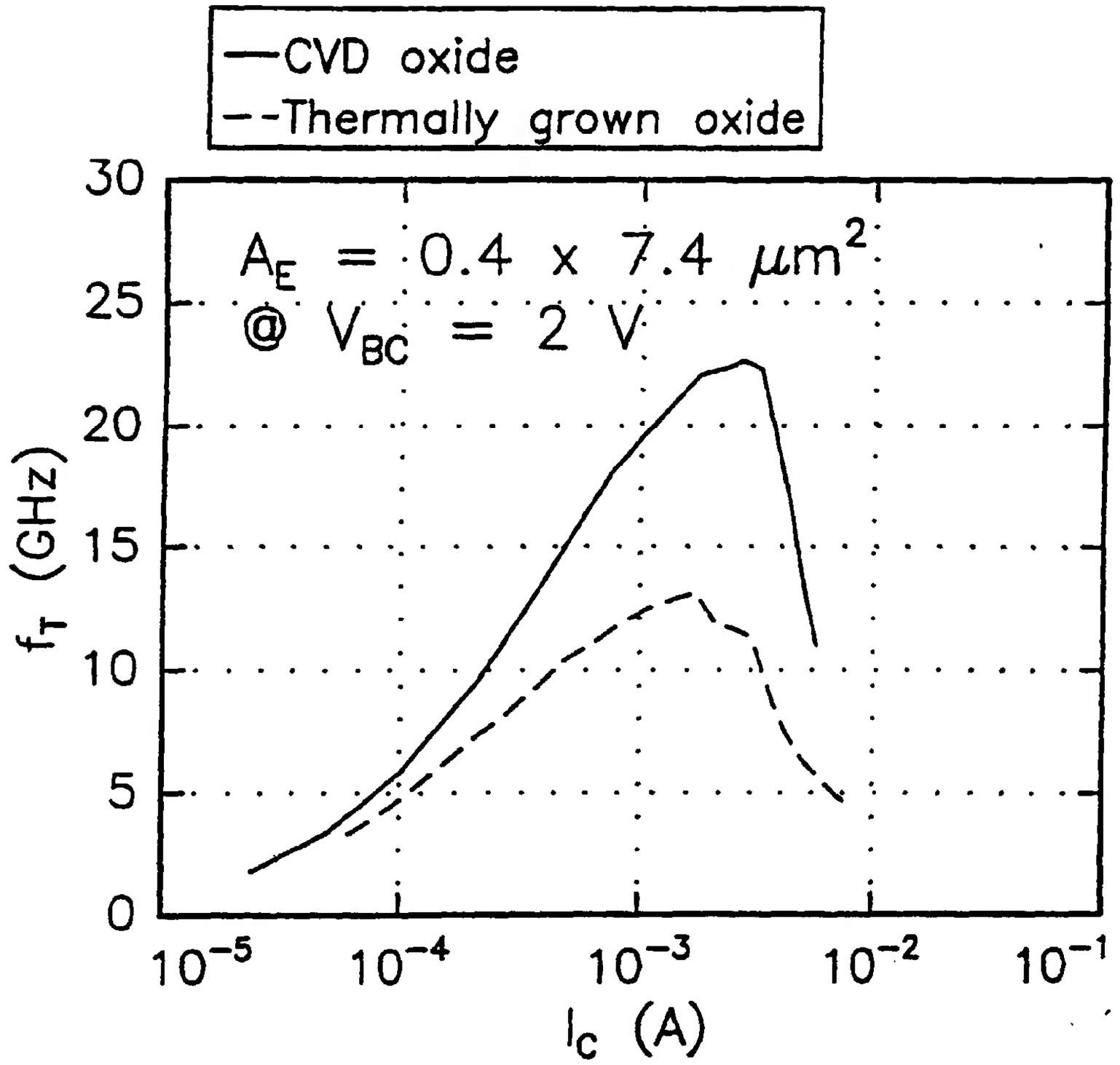

—CVD oxide
--Thermally grown oxide
A_E = 0.4 x 7.4 μm²
@ V_{BC} = 2 V
f_T (GHz)
30
25
20
15
10
5
0
10^{-5}
10^{-4}
10^{-3}
10^{-2}
10^{-1}
I_C (A)

FIGURE 14

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 83 0259

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	LOMBARDO S ET AL: "Ge ion implantation in Si for the fabrication of Si/Ge/sub x/Si/sub 1-x/ heterojunction transistors" MATERIALS CHEMISTRY AND PHYSICS, NOV.-DEC. 1996, ELSEVIER, SWITZERLAND, vol. 46, no. 2-3, ISSN 0254-0584, pages 156-160, XP002054913 * paragraph 2; figure 1 * * paragraph 4 * * paragraph 5 * ---	1,4,5,8, 10,11,13	H01L21/331
A	TAKAYUKI GOMI ET AL: "A SUB-30PSEC SI BIPOLAR LSI TECHNOLOGY" INTERNATIONAL ELECTRON DEVICES MEETING, SAN FRANCISCO, DEC. 11 - 14, 1988, no. 1988, 11 December 1988, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, pages 744-747, XP000014724 * page 744, right-hand column; figure 3 * ---	1,5,8,11	
A	PATENT ABSTRACTS OF JAPAN vol. 016, no. 130 (E-1184), 2 April 1992 -& JP 03 292740 A (HITACHI LTD), 24 December 1991, * abstract; figure 3 * -----	1,5,8,11	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	6 February 1998	Gélébart, J

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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